AROD VEHICLE TRACKING RECEIVER

FINAL REPORT AND INSTRUCTION MANUAL

CONTRACT NAS8-5483

NASA MARSHALL SPACE FLIGHT CENTER

157P

Prepared by

Astrionics Center

ITT Federal LABORATORIES

A DIVISION OF INTERNATIONAL TELEPHONE AND TELEGRAPH CORPORATION

15151 BLEDSOE STREET, SAN FERNANDO, CALIFORNIA

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15151 BLEDSOE STREET, SAN FERNANDO, CALIFORNIA

15151 Bledsoe Street

San Fernando, California

telephone EMpire 7-2211

ITT Federal LABORATORIES

Chicago
Fort Wayne
Palo Alto
San Fernando
Nutley

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1.0 INTRODUCTION

This document covers the final report and instruction manual for the "Brassboard" model of the AROD (Airborne Range and Orbit Determination) vehicle tracking receiver. The purpose of this receiver is to demonstrate the feasibility of the AROD system by flight tests in an airplane. Thus, the size, weight, and environmental requirements were less stringent for this piece of equipment than for one designed to be flown in a missile or satellite.

While it is not the purpose of this report to discuss the complete AROD system, a brief description is included to orient the reader to the purpose and general requirements of the vehicle tracking receiver discussed in this report.

AROD is a space vehicle guidance system based on trilateration with measurements of range and range rate from the vehicle to three or more fixed ground stations of known location. In the AROD system, the central station is located on the vehicle. It contains the usual category of equipment such as standard frequency generator, transmitter, receiver, demodulators, computer, and such auxilliary devices as are required to operate the system. Each ground station requires only a transponder which receives the signal emitted from the vehicle and sends back a coherent version of the received signal.

The AROD system will provide for simultaneous reception from four transponders, although only three stations need be received to completely determine the vehicle's position and course. The vehicle tracking receiver, therefore, is a four channel unit.

The determination of the range to each ground station transponder is made by measurement of the time delay between transmission of a signal from the vehicle to the ground station and reception of a signal returned from the ground station to the vehicle. In order to provide accuracy in this measurement, the phase delay of a high frequency sine wave modulated onto the transmitted carrier is measured. Since this measurement can be ambiguous if the vehicle is at a greater distance than one wave length of the modulating signal, additional lower frequency modulated signals are used, the lowest one determining the furthest distance at which a non-ambiguous measurement can be made. AROD uses modulation frequencies of 2.342 MHz, 73.1875 KHz, 2.287 KHz and 71.47 Hz in order to provide range measurement accuracies of ±1 meter at distances to over 4000 kilometers. The RF carriers are in the 2.2 KMHz band. The vehicle transmitter transmits a carrier modulated with the sidetone frequencies. These are received by the transponder and coherently displaced in frequency. There are four different displacements made to provide for four receiving channels. Figure 1-1 shows the relationships of the four carriers and their sidetones. As will be noted from Figure 1-1, the channels are

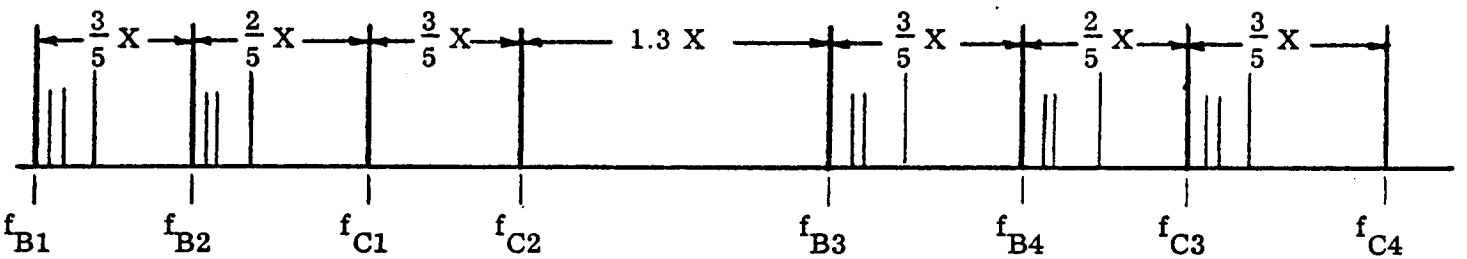
interleaved in order to conserve frequency spectrum. The range tones are single sideband amplitude modulated on their carriers.

Range rate is measured by means of the doppler shift of the received signal, which has on it a double doppler resultant from the round trip made by the signal, since the transponder does not remove the doppler from the signal received from the vehicle.

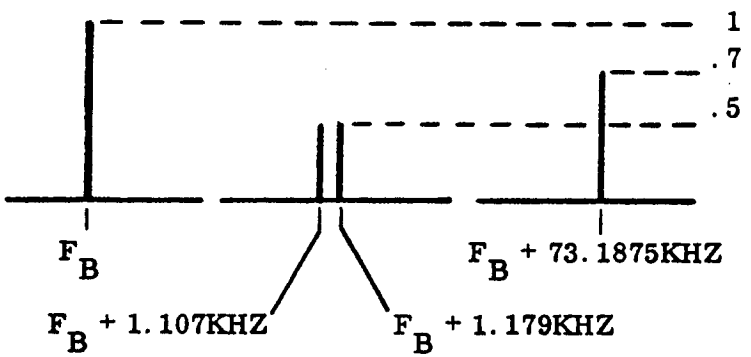
The vehicle tracking receiver must receive four channels simultaneously extract the range tones from each channel signal, and send them to the range data extraction unit at the proper amplitudes. Likewise the doppler frequency must be extracted and sent to the velocity data extraction unit.

In order that all frequencies involved are coherent, and accurate they are generated in a frequency synthesizer whose primary frequency source is a very stable oscillator. All local oscillator and reference frequencies, except the voltage controlled oscillators associated with phase lock loops are provided by the frequency synthesizer.

During the design of this receiver, consideration was given to the ultimate necessity of miniaturizing the product at a later date. Therefore, in many instances circuits which would permit easy microminiaturization were selected. An example of this is the use of video type broadband RF amplifiers, with appropriately located filters instead of using RF amplifiers with tuned circuits. Another example is the use of active type filters using twin T feedback networks for the audio frequency filters. (Later experience indicated the need for at least one of the audio filters to take the form of a phase locked loop in order to obtain a bandwidth narrow enough to remove all undesired signals.)



X = 2.342MHZ



Detail of Spectrum Near F_B

Figure 1-1. AROD Receiver Spectrum

2.0 RECEIVER DESCRIPTION

The vehicle tracking receiver is a four channel receiver. The input section is common to all four channels. The remainder of each channel is completely independent of all other channels.

2.1 General Description

The vehicle tracking receiver consists of a RF amplifier, first mixer, and a first i-f amplifier common to all channels. The output of the first i-f amplifier is split into four parts, one part feeding the second mixer of each channel. The ITTFL supplied part of this receiver starts with the first i-f amplifier, as shown in the block diagram of Figure 2-1. The output on each channel of the first i-f amplifier feeds the second mixer. This mixer receives its L.O. signal from the Voltage Controlled Oscillator (VCO) of the main (4.684 MHz) phase-lock loop. The output of the second mixer is filtered in two parallel crystal filters in order to reject the interleaved signals of the adjacent channel. This is possible, since the doppler is removed from the main carrier on each channel by the phase-lock loop, and only the small doppler associated with a frequency of 2.342 MHz is present on the modulation carrier. The second i-f amplifier provides the AGC action as well as a large share of the receiver gain. Since the VCO's of each channel are on the same frequency of 84.312 MHz, the second intermediate frequency of each channel is different. The pertinent signal frequencies for each channel are listed in Table 2-1

In order that a common frequency can be used for the phase detectors of each channel, a third mixer is used, converting the main carrier of the second intermediate frequency to 4.684 MHz. The phase-lock loop consists of the phase detector, the P.L.L. filter, the VCO, the second miser and its following i-f amplifiers and mixers. The phase-lock loop has a 100 Hz bandwidth which provides a high sensitivity of approximately -140 dbm for lock on.

The 2.342 MHz high frequency range tone is extracted by beating together the two carriers in the second i-f amplifier. This signal is then filtered by a phase-lock loop which also provides amplitude demodulation of the lower frequency side tones. In observing the spectrum of Figure 2-1 it will be noticed that no sidetones exist at 71.47 hertz or at 2.287 KHz. In order to eliminate the need for a low frequency sideband on the 2.342 MHz signal, the 2.287 KHz and 71.47 Hz signal are transmitted as two frequencies whose sum is 2.287 KHz and whose difference is 71.47 Hz. These signals are extracted by mixing the two frequencies and filtering out their sum and difference products. The 73.1875 KHz sidetone is extracted by filtering out this signal from the demodulated 2.342 MHz carrier.

TABLE 2-1

AROD VEHICLE TRACKING RECEIVER FREQUENCIES

Ch. No.	R.F. Main Carrier	1st IF Main Carrier	2nd IF Main Carrier	2nd IF Mod. Carrier	3rd IF Main Carrier
	MHZ	MHZ	MHZ	MHZ	MHZ
1	2211.8848	96.9588	12.6468	10.3048	4.684
2	2213.1900	98.3640	14.0520	11.7100	4.684
3	2218.5766	103.7506	19.4386	17.0966	4.684
4	2219.9818	105.1558	20.8438	18.5018	4.684

In order that each transponder may be properly identified during the acquisition period, a pulse modulation is applied to the 73.1875 KHz signal. This is demodulated in the vehicle tracking receiver and the pulse video is delivered to the command decoder for identification.

The "brassboard" receiver is packaged in five chassis, each measuring 7" high by 19" wide (standard rack panel) by 22 inches maximum depth. One chassis contains the RF amplifier, first mixer, first i-f amplifier and DC power supplies which are common to all four channels. Each of the other four chassis contains the remainder of the circuitry required for each channel. Due to funding limitations, only three channels were actually provided. .The fourth channel can be added at any time.

Each chassis is built in modular form. The common chassis contains two power supply modules and one first i-f amplifier module. In addition, the RF amplifier and first mixer assemblies will be added to the common chassis. They were not supplied by ITTFL.

2.1.1 1st I-F Amplifier

The first i-f amplifier provides 50 db of gain to the signals of all four channels of the Vehicle Tracking Receiver, and distributes its output signal to each channel.

The preliminary design of this amplifier showed that if resistive type isolation was used at the output of the active elements, the signal level required to be developed before division would be too high to be handled with normal receiving-type transistors without compression since no AGC is used in this amplifier. It was therefore decided to put one stage of amplification in each output leg in order to reduce the high level signal requirement.

Due to the mechanical layout required for the four output stages plus a fifth test output stage, some difficulty was encountered in obtaining an even distribution of output power and enough overall gain and inter-output isolation. Several methods of distributing the power to each output stage were tried, including the use of resistive dividers, capacitive dividers and half-wave length lines. None of these were successful. Finally the use of three lumped constant hybrid loops as a power divider solved the distribution problem to the four channel output stages. The test output stage was capacitively coupled through a very low value capacitor to the amplifier output stage.

The final design of this amplifier provided over 50 db gain and better than 50 db isolation between outputs. The test output has approximately 20 db less gain than the normal receiver outputs, but satisfactory operation of noise figure measurement equipment is obtained with proper auxilliary amplifiers.

Wideband video type amplifiers are used not only for this amplifier, but also wherever else possible in this receiver in order to provide a linear phase characteristic. The phase characteristics are therefore determined essentially by the filters.

2.1.2 2nd Mixer and Filter

The 2nd mixer has as its inputs the first i-f signal and the VCO signal.

The output of this mixer is split and fed to two crystal filters in parallel. The center frequencies of these two filters are separated by 2.342 MHz as are the two equal amplitude main signals of each channel. The highest frequency filter for each channel, centered respectively at 12.6468, 14.0520, 19.4386 and 20.8438 MHz passes the carrier to which the first phase-lock loop is locked. Since this carrier is always maintained at the i-f center frequency and has no modulation on it, the bandwidth of these filters is narrow, being ±10 KHz. The lower frequency carrier has on it the ±160 Hz doppler, and the 73.1875 KHz, 1.179 and 1.107 KHz sidebands. To accommodate these sidebands, the bandwidth of the lower frequency filter is ±100 KHz.

Since the sidebands appear only on the high frequency side of their carrier, the filter bandwidth could be narrower, which would result in about 3 db less noise getting into the i-f. However, it was felt that in the interest of phase stability, the carrier should appear at the center of the filter, so the wider bandwidth was chosen.

The outputs of the two filters are combined through a resistance adding network. A two stage broadband video type amplifier provides gain to compensate that lost through the filters and the adder. The overall gain of the module is nominally zero db.

2.1.3 2nd I-F Amplifier

This amplifier includes a t-stage tetrode transistor amplifier with AGC on each stage. The total AGC range is greater than 60 db. Type 3N35 tetrode transistors are used in a circuit which permits compensation of the phase shift with change in AGC voltage. The AGC voltage is applied to both the base two and the emitter of the tetrode transistor through suitable resistor networks. By adjusting the ratio of AGC applied to the base two and emitter, the change in transit time with AGC voltage can be made to compensate for the change in phase caused by circuit detuning. Since this amplifier is of the broadband video type without tuned circuits, the change in phase due to effective output capacitance change will be small, so that only a small change in transit time is required. Due to funding limitations no actual measurements of the change in phase of this amplifier with AGC were made. It is anticipated that this will be done on the overall receiver by the systems integration contractor.

The 5-stage amplifier is followed by a filter of about 4 megacycles bandwidth to limit the noise to levels so that they are within the dynamic range of the following amplifiers. This filter is of the pi network type which provides a high degree of phase linearity across its passband. Two additional stages of amplification are provided to bring the net gain of this module to about 50 db.

At this point the signal is split. One portion goes to the third mixer where it is converted to 4.5 MHz. The other portion is further amplified and fed to a diode rectifier. The DC output of this rectifier is used as a non-correlated AGC and is normally set to hold the output signal level 20 db higher than the correlated AGC level. This diode rectifier also acts as a mixer in which the two main signals, located 2.342 MHz apart beat together to produce the 2.342 MHz range tone signal.

There are two possible methods of developing this 2.342 MHz range tone signal. Each has advantages and disadvantages. By mixing the two signals together as is being done in this receiver, the phase relationship between the two carriers is preserved. However, the threshold of efficient detection appears to be at a signal-to-noise level of about -15 dbm into the diode detector. Also, the output signal level from this diode detector varies over the dynamic range of operation. This can be overcome by the use of a separate AGC control on the 2.342 MHz signal. The implementation of such an AGC will not be difficult, since the correlation detector output of the phase-lock loop used to filter the 2.342 MHz signal provides a voltage to control the AGC. If the diode detector continues to be used in future receivers, it is strongly recommended that such an AGC control be added. With sufficient gain in the 2.342 MHz signal path, and using amplifiers of great enough dynamic range, it should be possible to make this method operate satisfactorily at input signal levels as low as -130 dbm.

The other method of obtaining the 2.342 MHz signal is to replace one of the received signals by a locally generated clean signal. In this manner, the 2.342 MHz signal can be generated at input signal levels as low as that to which the receiver main phase-lock loop will remain locked. The incoming signal is kept in phase with the locally generated signal through the main phase-lock loop. However, there is a phase error present which is that required by this phase-lock loop to track the signal. By the use of a modified third order loop, this error is kept below 5 degrees. Still it is a source of error in the measurement. So a compromise must be made as to whether it is better to eliminate this source of error and have a lower useable sensitivity of the receiver, or to involve in the measurement the tracking error of the phase-lock loop, but in so doing, be able to operate at a lower value of input signal level. Since receiver noise begins to be an appreciable source of error at input signal levels

below -130 dbm it is recommended that the diode detector be retained, with AGC of the 2.342 MHz signal added.

2.1.4 AGC Circuits

A high-gain AGC loop is used in this receiver. The output of the main loop correlation detector varies less than one-quarter of a db over a signal input range from -140 dbm to -90 dbm into the first i-f amplifier. At signal levels below -140 dbm the correlation output drops off less than 3 db to the point where lock is lost.

The input to the AGC amplifier is a diode switch which automatically selects the correlated AGC source or the uncorrelated AGC source according to which output is the most negative value. This assures that the correlation output will take over and hold the receiver i-f output to the phase detector at the proper value to provide the required phase-lock loop bandwidth. The output of the AGC amplifier drives two emitter followers. One of these provides the AGC voltage to the i-f stages; the other provides a monitor voltage to telemeter the AGC level.

The AGC time constant has been selected at 300 milliseconds for the AGC buss to reach 90% of its final value after a 6 db step change in input, which does not cause overload of the receiver circuits. This value was selected as a reasonable compromise which will be satisfactory under the usual operating conditions, since no selection of the time constant is provided. Actually, this value will change some with signal level, since the AGC loop gain is not constant with changes in signal level. This is due to the fact that the AGC vs dbm signal level is not a straight line but becomes flatter as the input signal level increases. Thus the gain of the AGC loop is higher at higher input signal levels which reduces the time constant.

Upon acquisition, when the gain control switches from the non-correlated to the correlated AGC, it may require several seconds for the AGC to settle out to its final value. If this is objectionable in system operation, it may be necessary to shorten the AGC time constant. A value of 50 to 100 milliseconds may be a good compromise under this condition.

2.1.5 Third I-F Mixer and L.O. Signal Generator

The original design of the receiver called for the phase detector frequency to be equal to that of the second i-f amplifier. This required the phase detector to operate at frequencies from 10 to 20 MHz. While it is quite probable that, with sufficient time, a satisfactory phase detector operating at these frequencies could be developed, it was felt that in view of the short time scale involved, it was better to use the 4.5 MHz phase detector which ITTFL had already developed. This then

required a third conversion of the intermediate frequency to a frequency close to 4.5 MHz. Since a 4.684 MHz reference frequency was available from the frequency synthesizer, this was chosen as the 3rd intermediate frequency.

Since the synthesizer also puts out a frequency equal to that of the second intermediate frequency on each channel, it was decided that this signal would be mixed with the 4.684 MHz to produce a L.O. frequency 4.684 Mhz below the 2nd intermediate frequency to be used as an L.O. signal for the third mixer. While this appeared simple, there were problems of keeping the coherent 4.684 Mc signal from entering the i-f channel through the mixers, or from stray coupling. One problem was due to the high (+10 dbm) level of these signals from the frequency synthesizer. The first module built proved to have excessive correlated reference signal in the i-f output, and a relayout of this module was made, using a separate shielded compartment for developing the L.O. signal from the two reference signals. At the same time the level of the reference signals brought into the module was reduced by 10 db. The levels of these reference signals were further attenuated inside the module with the result that the level of undesired reference signal in the i-f output was acceptably low.

In the L.O. signal generator section, the attenuated input reference signals are fed into a balanced mixer. Since neither of these signals is high enough in level to saturate the mixer, its output level is dependent upon the input level of both signals. However, the output signal level of the frequency synthesizer will be constant, so no ill effects should be noticed from this. In fact, this provides a method of gain control which will be discussed later.

The signal from the second i-f amplifier is filtered with a bandpass of ±700 KHz to remove the lower frequency signal and its sidebands. It is then converted to 4.684 MHz in a balanced mixer. Another L-C filter with a ±500 KHz passband follows the mixer to remove any of the L.O. signal which might get through the balanced mixer. The output of this filter is split to feed two identical output amplifiers. One of these feeds the phase detector. The other output was provided to drive a discriminator as an acquisition aid. The acquisition aid circuit was eliminated from this procurement, but the output was retained in case it is later decided to add the discriminator. In the meantime, this output makes a useful test point.

While originally conceived to have unity gain, this circuit actually supplies from 8 to 15 db gain, depending upon the level of the higher frequency reference signal supplied to the signal generator signal. Because of this, it is possible to use the gain variation of this circuit to control the level of the 2.342 MHz signal output of the second i-f amplifier module. Since the AGC system holds the level of the received

signal to the phase detector constant, the output level of the 2nd i-f amplifier will be determined by the gain of the 3rd mixer circuit. The level of the 2.342 MHz signal is determined by the output level of the 2nd i-f amplifier. Hence the 2.342 MHz output level can be controlled by adjusting the higher frequency reference voltage level to the L.O. signal generator circuit. It should be noted that the 4.684 MHz reference signal must be held at a level between -2 dbm and 0 dbm as this signal is also fed to the phase detector. If the level of this reference signal falls much below -2 dbm, the dynamic range of the phase detector will be reduced.

2.1.6 4.684 MHz Phase Detector

The 4.684 MHz phase detector uses essentially the same module as is used in the ITTFL Model 4003 Autotrack Receiver. The circuits of this phase detector tune to 4.684 MHz without any changes required. The only change made in this module to adapt it to the AROD receiver was to eliminate two auxilliary output amplifier stages, which were not required.

This phase detector module contains two identical phase detectors with amplifiers on both the signal and reference inputs of each to provide the proper drive and isolation. The phase detector itself consists of a double diode quad bridge providing full-wave detection. The DC balance of these phase detectors remains within 1% of the nominal maximum output, and is typically less than ±2.5 millivolts.

Isolation is provided in both the reference and signal input leads between the two phase detectors in this module. The reference signal to one phase detector is shifted by 90 degrees with respect to the reference signal to the other phase detector. This allows one to become a correlation detector while the other acts as a phase detector. A potentiometer adjustment of this phase shift is provided.

The nominal value of reference signals to this module is 0 dbm, although it can be operated with -2 dbm reference signal with negligible degradation of performance. The nominal value of i-f signal required by this module is -30 dbm, or 7 millivolts RMS into 50 ohms, which produces an output of 0.25 volts per radian phase error near the zero output region. Due to the sine function characteristic, the maximum DC output of the correlation detector is ±0.25 volts with -30 dbm input level. This output is amplified by an operational amplifier whose gain can be adjusted from unity to about 90. However, the output of the operational amplifier limits at values of 12 to 14 volts. In the AROD receiver the gain is set to a value of approximately 16, providing a nominal DC output of -4 volts.

The dynamic range which the i-f signal amplifiers in this phase detector can accommodate is 26 db. Since peak noise to peak signal ratio is in the order of 6 db, this phase detector can accommodate without

clipping, a noise level 20 db above the signal level. This means that for maximum performance the i-f bandwidth ahead of the phase detector should be limited to 100 times the phase-lock loop bandwidth, or for a 100 Hz loop bandwidth the i-f bandwidth should be 10 KHz (±5 KHz). However if an additional crystal filter must be used to provide this bandwidth, the steep phase slope of the combination of this filter and the ±10 KHz crystal filter following the 2nd mixer can produce an unstable condition in the loop which prevents the loop from locking to the signal. To prevent this, the bandwidth of the i-f amplifier has been limited only by the ±10 KHz crystal filter following the 2nd mixer. The phase-lock loop will remain locked at signal levels of -140 dbm or lower.

2.1.7 4.684 MHz P.L.L. Filter

The 4.684 MHz or main phase-lock loop includes the 2nd mixer, 2nd i-f amplifier, 3rd mixer, phase detector, filter and VCO, including the frequency multiplier of the VCO module.

This loop is of a modified third order design. By separating the break frequencies of the passive and active filters in the loop, a considerable gain in loop stability is obtained with only a slight degradation of performance. In the AROD system, a very low order of both static and dynamic phase error is required when following high rates of doppler shift so as to not introduce errors into the measurements.

The P.L.L. filter used is essentially a copy of the filter used in the ITTFL Model 4003 Autotrack Receiver, with changes in the resistor values as required because of the difference in VCO sensitivity. Another change made was the substitution of the Philbrick Model PP65A operational amplifier for the larger Model P2 amplifier. The PP65A amplifer, however, has a lower input impedance than the P2, which limits the impedance allowable in the passive filter. To provide the required loop bandwidth of 100 cps, the passive filter series resistance is 115 K ohms which is satisfactory for use with the PP65A amplifier.

The tuning circuit used with the third order loop enables the tuning voltage to be removed from the loop after acquisition without causing a transient. Due to the necessity of removing any bias from the tuning control voltage, the actual switching is performed by a relay, rather than a solid state switch. This relay also operates a front panel indicator lamp to show that the loop is locked. A monitor output point to telemeter the in-lock condition is also provided.

2.1.8 Acquisition Circuits

The acquisition circuit is required to remove the tuning voltage from the phase-lock loop when acquisition has been accomplished. Upon acquisition, the correlation detector produces a negative output voltage.

This voltage is filtered and amplified. It then operates a relay to remove the tuning voltage. While the use of relays in high reliability devices is to be avoided as much as possible, the requirement exists here that the tuning voltage be applied or removed without a DC offset and that in the open state, an extremely high resistance be maintained. Due to the limited time scale available, the relay was the logical choice for the "brassboard" model. However, if possible, a solid state type of switch should be developed for this purpose.

The acquisition circuits for both phase-lock loops are identical.

2.1.9 Signal-to-Noise Ratio Detector

Since the AGC of the receiver keeps the signal output of the i-f amplifier at a constant value, the measurement of the signal-to-noise ratio can be accomplished by a measurement of the noise level.

Receiver input noise is contained with the frequency band between the modulated carrier and its 73.1875 KHz sideband. This noise is present in the output of the 2.342 MHz signal developed by mixing the two main signals of the channel. The region at 2.305 MHz, which is half-way between the 73.1875 and the 1.179 KHz sidebands was chosen as a good region to sample the noise.

A crystal filter is used to pass only a 7 KHz wide region which contains the desired noise components. This noise is then amplified in a two-stage tuned amplifier since phase response is not important. The output of the amplifier is detected by a diode rectifier. The rectified noise output after filtering is available at a monitor point for telemetering. An emitter follower is used to provide a low impedance output. This DC voltage is also used to operate a Schmitt trigger which provides a positive output voltage whenever the signal-to-noise ratio falls below a predetermined point. This point is adjustable over a range representing a signal-to-noise ratio in the 100 Hz phase-lock loop bandwidth of 10 to over 40 db.

2.1.10 VCO

Upon recommendation of the contracting agency, a Damon Engineering Corp. crystal controlled VCO was used. This unit was purchased to specifications of less than 250 cycles drift per year. However, the units actually received exhibited considerably greater drift, as much as 1 Kc over a two week period. However, after an initial drift, the units seemed to settle down to a lower rate of drift. No actual measurement of this drift was made.

The VCXO is at 10.539 MHz. The output frequency is quadrupled and then doubled to 84.312 MHz. All of the circuitry is straightforward. Two

isolated output amplifiers provide separate outputs for the second mixer L.O. and the doppler detector.

The VCO was specified to have a sensitivity of 3 KHz per volt (at 10.539 MHz). The units received actually had a sensitivity of 2.2 KHz per volt. This required about ±9.1 volts swing instead of the anticipated ±6.7 volts to cover the ±160 Mhz range. It was agreed with the contracting agency that if the VCO could be swung ±140 Khz, it would be adequate for the tests envisioned. Accordingly the calibration of the front panel frequency meter was made ±150 Khz, which fitted the scale nicely. However, it was found that on all of the channels, the VCO could be pulled to the ±160 KHz originally requested, which causes the front panel frequency meter to go off-scale. This should not damage the meter as the overload cannot exceed 150% of full scale due to limiting in the driving amplifiers, nor can such overload be suddenly applied.

2.1.11 Doppler Detector

The doppler detector not only extracts the doppler frequency from the VCO output, but also multiplies this frequency by a factor of ten.

The VCO input frequency of 84.312 MHz plus or minus the doppler frequency is mixed with a 70.260 MHz standard frequency signal supplied by the frequency synthesizer to produce a signal of 14.052 MHz plus or minus the doppler. This 14.052 MHz signal is then multiplied by factors of five and two to produce a frequency of 140.52 MHz plus or minus ten times the doppler. This signal is mixed with a 140.52 MHz standard frequency signal supplied by the frequency synthesizer to produce a signal of ten times the doppler signal. Since this signal will go through zero frequency, it would be necessary to provide DC coupling of the output. In order to eliminate the need for DC coupling, a low frequency of 2.5 Hz was chosen as the 3 db cutoff frequency, which considerably simplified the required circuitry.

One doppler detector is required for each channel. However, only one output of the 70.26 and 140.52 MHz signals was provided on the frequency synthesizer. In order to enable the four channels to use the single output, the reference signals are routed from the doppler detector of one channel to the doppler detector of the next channel. Two connectors are provided on each channel chassis for each of these two signals. It is necessary that each of these lines be finally terminated in 50 ohms. Therefore, the last chassis to receive these reference frequencies will have the output jack terminated with a 50 ohm load.

Within the doppler detector module, the reference signals are taken off of the supply line with a high impedance which provides very light loading of the supply line, so that essentially equal power is available to each doppler detector. It also provides good isolation between doppler detectors of the four channels.

2.1.12 2.342 MHz Phase-Lock Loop

The 2.342 MHz phase-lock loop consists only of a phase detector, filter, and VCO. The VCO signal is used as a reference signal for the phase detector, so that the VCO tracks the incoming 2.342 MHz signal. Thus, the VCO frequency and phase is a replica of the incoming signal, but stripped of its modulation and most of its noise, due to the narrow bandwidth of the phase-lock loop. A slight error required to keep the loop in lock exists between the phase of the VCO and the incoming 2.342 MHz signal. Due to the use of a third order loop, the phase error required to statically or dynamically follow the signal is less than one degree. However, this is about one-third of the total error with which the phase must be measured in order to meet the anticipated range measurement accuracy of ±1 meter.

The VCXO is a Damon Engineering Corp., crystal voltage controlled oscillator, operating at 2.342 MHz. The output of the VCXO is split with resistance isolation networks to supply two output stages. One of these supplies an output signal level of +10 dbm at 50 ohms impedance to the range extraction unit. The other supplies an output signal level of 0 dbm at 50 ohms to the phase detector.

The phase-lock loop is a modified third order loop with a tuning circuit similar to that used in the main phase-lock loop. In order to provide acquisition of a signal as much as 400 cps from the nominal VCO frequency, the phase-lock loop has a bandwidth of 100 Hz when in the unacquired state. However, as soon as the correlation detector provides a sufficient output signal, a relay operates to narrow the bandwidth to 10 Hz. Since this change in bandwidth required a change in the passive filter resistance, which is in the DC input circuit to the operational amplifier, it was necessary to provide a separate path through which the DC input current, required at zero input voltage, could be supplied. This then allowed the filter resistance to be changed without introducing a zero shift in the operational amplifier output. In order that the impedance of this path does not appreciably load the passive filter, the bias current circuit consists of a very high value resistor (15 megohms) fed from an adjustable source of voltage. In order that the adjustment range could be kept small enough to enable a fine adjustment of voltage to be made, the range of voltage required had to be tailored to each operational amplifier.

To switch the bandwidth of this filter, a four pole relay was originally used as it was believed that several of the filter elements would require changing. However, it was later determined necessary to switch only one element of the filter which, with switching the tuning voltage, required only a two pole relay. However, the four pole relay was left in the circuit.

2.1.13 2.342 MHz Phase Detector

The 2.342 MHz phase detector, except for frequency, is identical with the 4.684 MHz phase detector. It was necessary only to change the tuned circuits. The correlation detector of this module provides the amplitude demodulation of the 2.342 MHz signal, producing the 1.107, 1.179, and 73.1875 KHz frequencies. In order to increase the amplitude of these frequencies as well as to provide a low impedance (500 ohm) source, an amplifier is provided. A gain control was also provided so that the proper level of signal could be obtained at this output.

2.1.14 Range Tone Extraction Circuits

The range tone extraction circuits filter out the 73.1875 KHz range tone, develop and filter the 2.287 KHz and 71.47 Hz range tones. The input signal is the demodulated spectrum from the 2.342 MHz carrier. The input signal is divided, one portion going to a 73 KHz filter having a 4 KHz bandwidth, and the other part going through a low-pass filter to a demodulator. The low pass filter removes the 73 KHz signal from the demodulator input.

The output of the demodulator consists mainly of six frequency components, which are the 1.107 and 1.179 KHz signals, their sums, differences, and second harmonics. Smaller amounts of other harmonics and intermodulation products are also present. The desired signals of 71.47 Hz and 2.286 KHz are filtered through two separate filters, each consisting of amplifier stages with twin T feedback networks. While from the standpoint of the frequency band needed to be passed, both of these filters could be of a 1 Hz bandwidth, from the phase response standpoint, a considerably wider bandwidth, such as 50 Hz is required in order to prevent an appreciable shift in phase as the frequency changes. Since the ratio of sidetone frequencies used for range ambiguity removal is 32, the phase must be determined with an accuracy of better than 32/360 or roughly, 10 degrees, which would be ±5 degrees from the true reading. Therefore, no more than about 2 degrees can be permitted for variation of phase due to the filter phase slopes.

A difficulty arises in the 2.287 KHz filter because of the second harmonics of the two detected signals being only ±71 Hz from the 2.287 KHz signal. Since these signals at ±71 Hz must be suppressed by at least 40 db, it is impossible to do this with a conventional filter without producing an unacceptable phase shift across the bands. However, a phase-lock loop filter would permit a bandwidth of a fraction of a Hertz and yet require less than one degree of phase error to follow the signal. Since this requirement was not realized until late in the program, time and funding did not permit a change to a phase-lock loop filter. However, if the zero crossing point is used in the range extraction unit, it may

be possible to live with this output as is. If not, it will be necessary to add a phase-lock loop filter to this output.

No problem presented itself in the extraction of the 71.47 Hz signal.

The 73.1875 KHz signal, after filtering through the 4 KHz wide filter has had considerable noise, as well as other unwanted signals removed from it. This signal is again split, with one portion going through another 73.1875 KHz filter, this one having a bandwidth of ±50 Hz. The output of this filter is amplified and becomes the 73.1875 KHz range tone signal. The other portion of the first 73.1875 KHz filter output is detected in a diode detector to obtain the pulse code modulation. In order to minimize noise riding on these pulses, the video amplifier is designed to clip the signal. This results in flat tops and bottoms to the pulses, but the rise and fall points are moved by the noise on weak signals.

Separate output level controls are provided on each of the three range tone outputs as well as the pulse video output.

2.2 Detailed Module Description

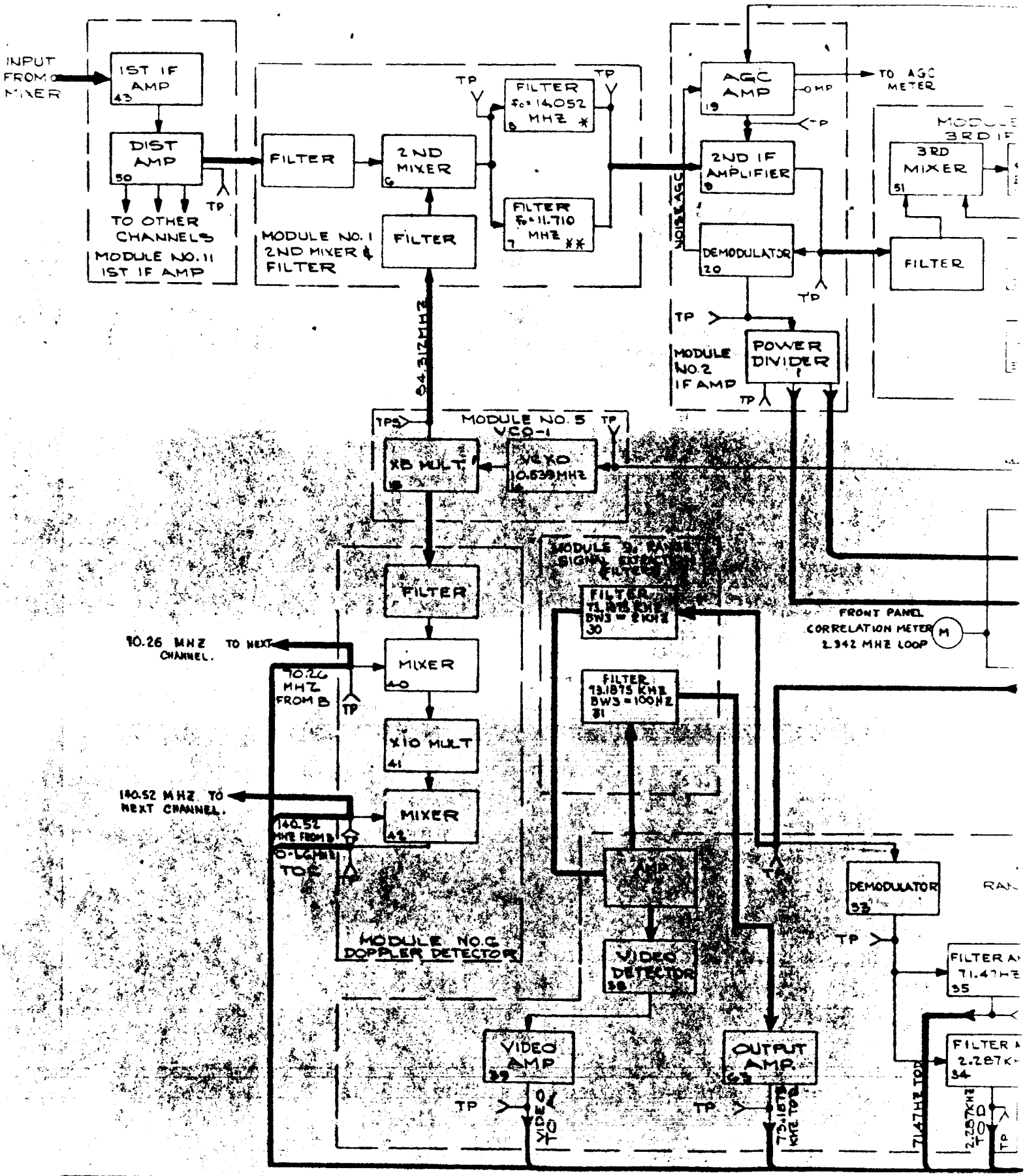
The following sections describe in detail the function and operation of each module in the receiver, using block diagrams and schematics.

2.2.1 First I-F Amplifier Module

Refer to Figure 2-2 for a block diagram of the 1st i-f amplifier module. Refer to Table 2-2 for target specifications and to Figure 8-2 for schematic of this module. One unit is used to supply all four channels.

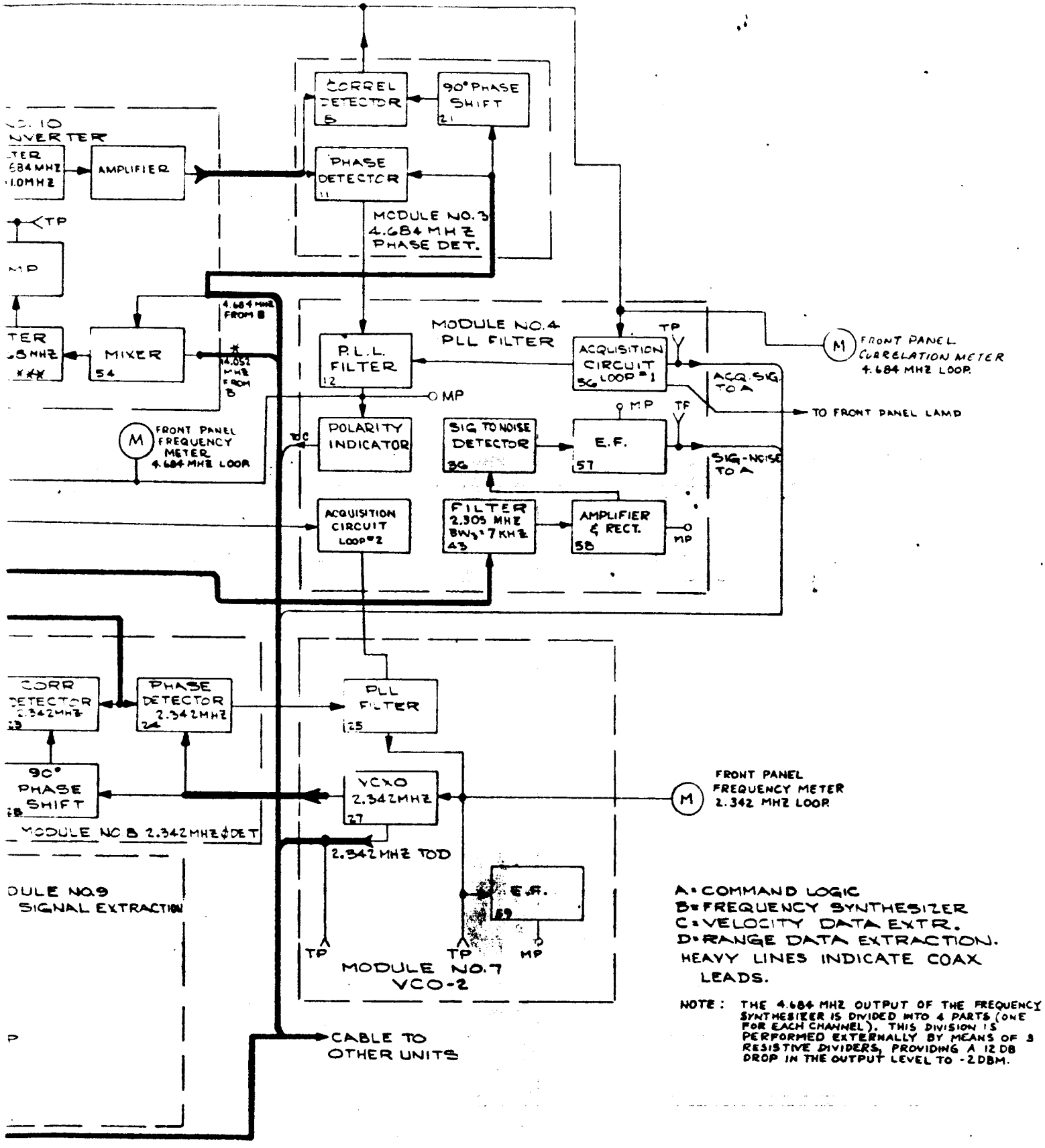
The basic purpose of this module is to amplify the incoming signals, all eight of them, and to distribute them equally to all four channel systems. Some frequency discrimination is provided in individual channel outputs in order to reduce the total spectrum power delivered to any one channel. Therefore, each output favors one particular channel and provides some attenuation for undesired channels. About 70 db of back isolation is provided in each channel output to insure no cross channel interference due to backward isolation path via L.O. chain, etc. All channels have equal outputs in pairs of signals. The first section of this module is very broadbanded to insure good linear phase response over the passband.

The eight combination of input signals together with their modulation sidebands are applied to J-1 from the first mixer. A pi coupling network is used to couple the input to a transistor amplifier using a 2N2398. The output of the amplifier is fed to a filter (LC - 5 section Pi)



CHANNEL NO.	INPUT	*	**	***
CHAN 2 (AS SHOWN)	24.022 MHZ	14.052 MHZ	11.710 MHZ	9.368 MHZ
CHAN. 1	28.344 MHZ	12.6468 MHZ	10.3048 MHZ	7.9628 MHZ
CHAN 8	28.2156 MHZ	19.4586 MHZ	17.0966 MHZ	14.7546 MHZ
	101.2856 MHZ			
	103.7856 MHZ			

FIG. 2-1 BL



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with a 30 MHz BW_3 centered at 100 MHz. This passes 85 to 115 MHz signals. The filter output is fed to a three-stage video amplifier using 2N2398 transistors. The output of the last video amplifier is coupled to a power divider through a pi network and is also lightly coupled to a test output stage.

The power divider, a hybrid type, distributes the power equally to 4 output amplifiers using 2N2398 transistors. Each stage is coupled to an output jack using a pi network coupling device to obtain proper impedance level and each pi network is tuned to the center of the desired channel. The test output uses similar devices but is much broader in order to allow all signals to be passed.

Microdot connectors are used throughout for signal connections and the chassis uses standard components with no printed boards. The power divider is built on a vector board and mounted in the center of the chassis.

2.2.2 Second Mixer Module (A1)

Refer to Figure 2-3, 2-4 and 2-5 for block diagrams of the Second Mixer and Filter Module. Refer to Table 2-3 for target specifications and Figure 8-6, 8-7 and 8-8 for schematics of this module. The basic purpose of this module is to convert signals in the 95 to 105 MHz range to signals in the 10 to 20 MHz range. It is not intended to provide gain in this module. All input signal and output signal connections are designed for 50 ohm circuits. All channels require the same local oscillator frequency, 84.312 MHz.

The input signals, which are different combinations for each channel, consist of two equal amplitude signals 2.342 MHz apart with the lower frequency one containing modulation sidebands, fed to input connector J1. An LC filter is provided consisting of 5 pi sections. This type of filter provides very linear phase response when aligned properly. The 3 db bandwidth is approximately 5 MHz. The filter provides partial isolation to signals of other channels thus reducing the input power of signals of other channels to the balanced mixer.

A second LC filter is provided which is also a 5 section pi filter and with a narrow bandwidth. This filter is placed in the L.O. input and passes 84.312 MHz but rejects the input signals. This provides isolation of channels through the L.O. feed system.

Signals from both filters are fed to a balanced mixer stage. The balanced mixer is a transistor mixer using two 2N2398 transistors. A balancing potentiometer is provided in both bias circuits to allow each mixer to be aligned for maximum rejection of input signals at the parallel collector circuit. These potentiometers can be optimized for conversion

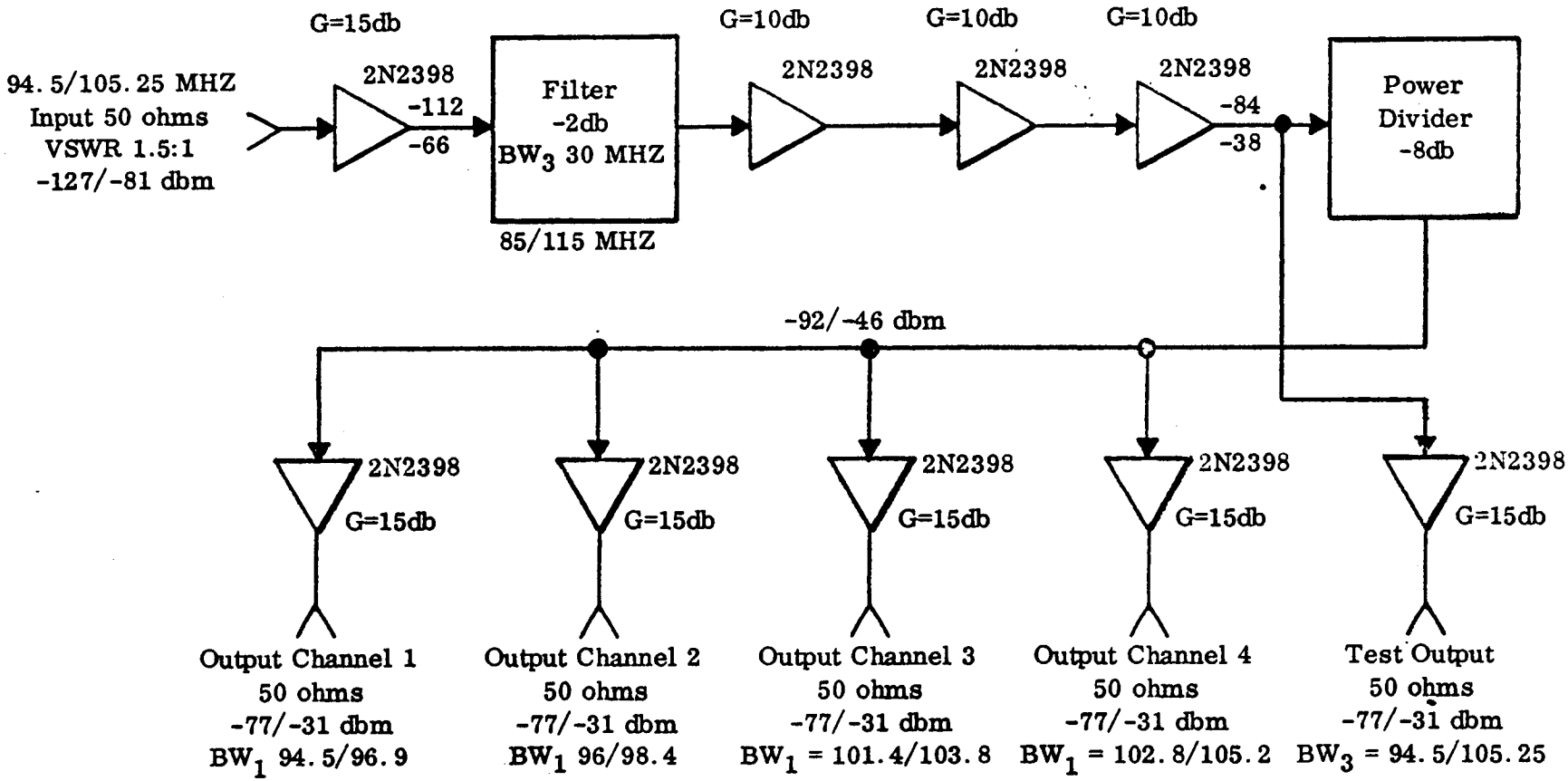


Figure 2-2. Block Diagram - 1st IF Amplifier

TABLE 2-2

SPECIFICATION FOR 1ST I-F AMPLIFIER MODULE

1.	Input Frequency:	94.5 MHz to 105.25 MHz
2.	Tuning Range:	Fixed
3.	Bandwidth (-3 db):	25 MHz minimum 26% BW 87 to 113 MHz
4.	Noise Figure:	7 db maximum 5 db design goal
5.	Gain:	50 db ±2 db (Need 40 db)
6.	Phase Characteristics:	±1% from linear ±13 MHz (Goal) (Range in Item 11)
7.	Input/Output:	50 ohms (VSWR 1.5:1)
8.	Input/Output Connectors:	Microdot 31-50
9.	Input Signal Level Range:	-127 to -81 dbm (includes peaking factor)
10.	Output Signal Level Range:	-77 to -31 dbm (no compression)
11.	Output Band Pass:	-1 db each Channel: Channel 1 - 94.5/96.9 MHz Channel 2 - 96/98.4 MHz Channel 3 - 101.4/103.8 MHz Channel 4 - 102.8/105.2 MHz Test Output - 94.5/105.25 MHZ (BW_3)
12.	Power Input:	+18 VDC @ 50 ma -18 VDC @ 50 ma DE9P Connector
13.	Size: Weight:	2 3/4" high x 3 7/8" wide x 9 1/2" long 3 lbs.
14.	Temperature:	25° C ±10° C minimum 0° C to 60° C design goal

gain as well as for balancing. Test point TP-2 is provided on the output of the mixer. The mixer output is divided in a passive resistance divider and is fed to two parallel crystal filters. Isolation between filter inputs as well as outputs is necessary to allow normal filter response and linear phase response. The crystal filter outputs are combined in a second passive resistance network and then fed to a two-stage video amplifier. The video amplifier is necessary to recover the losses incurred in the filters and the passive isolation networks. Two 2N2996 transistors are used for this purpose. Each channel block diagram shows the output frequencies. The higher frequency signal will be 2 db higher in amplitude to compensate for gain drop-off in the next module. A test point, TP-1, is also provided for output monitoring. Microdot connectors are used throughout for signal connectors. Separate partitions are used for shielding filter sections of the input filters. Printed boards are used for active circuits. Crystal filters use a temporary mounting arrangement for the original modules.

2.2.3 2nd I-F Amplifier Module

Refer to Figure 2-6, 2-7, 2-8 for block diagrams of the 2nd I-F Amplifier Module. Refer to Table 2-4 for target specifications and to Figures 8-9, 8-10 and 8-11 for schematics of this module. The basic purpose of this module is to provide 50 db of amplification and an AGC control range of better than 40 db. This module also provides a detector circuit with two purposes; first to supply the 2.342 MHz signal developed from both of each channel's carriers and secondly to provide an uncorrelated AGC voltage, which sets the sensitivity of the system with no signal applied. A gate is also provided to allow correlation AGC takeover upon lock-on during system operation.

Each channel's block diagram or the schematic shows the input frequencies which are fed to J-1. This input is swamped with a 100 ohm resistor whose function is stabilization and to maintain a VSWR less than 1.5:1 over the required frequency range. Five cascaded video amplifiers follow, using 3N35 tetrode transistors. These stages provide a gain overall of 40 to 50 db depending on the frequency. A phase compensation control R-1 is provided to allow constant phase response adjustment over the dynamic AGC range.

Since the tetrode amplifiers are very broad, a large noise spectrum occurs which detracts from the dynamic range of the following amplifiers especially because of the low frequency noise spectrum present. Therefore, a bandpass filter is provided which has a 5 MHz bandwidth at the -3 db points. This limits the noise spectrum to a tolerable level of power. The filter feeds a two-stage video amplifier and its output is connected to J-3. Negative feedback is incorporated into this amplifier to maintain more even gain response and stability. A 100 ohm swamping resistor is used to maintain VSWR 1.5:1 or less.

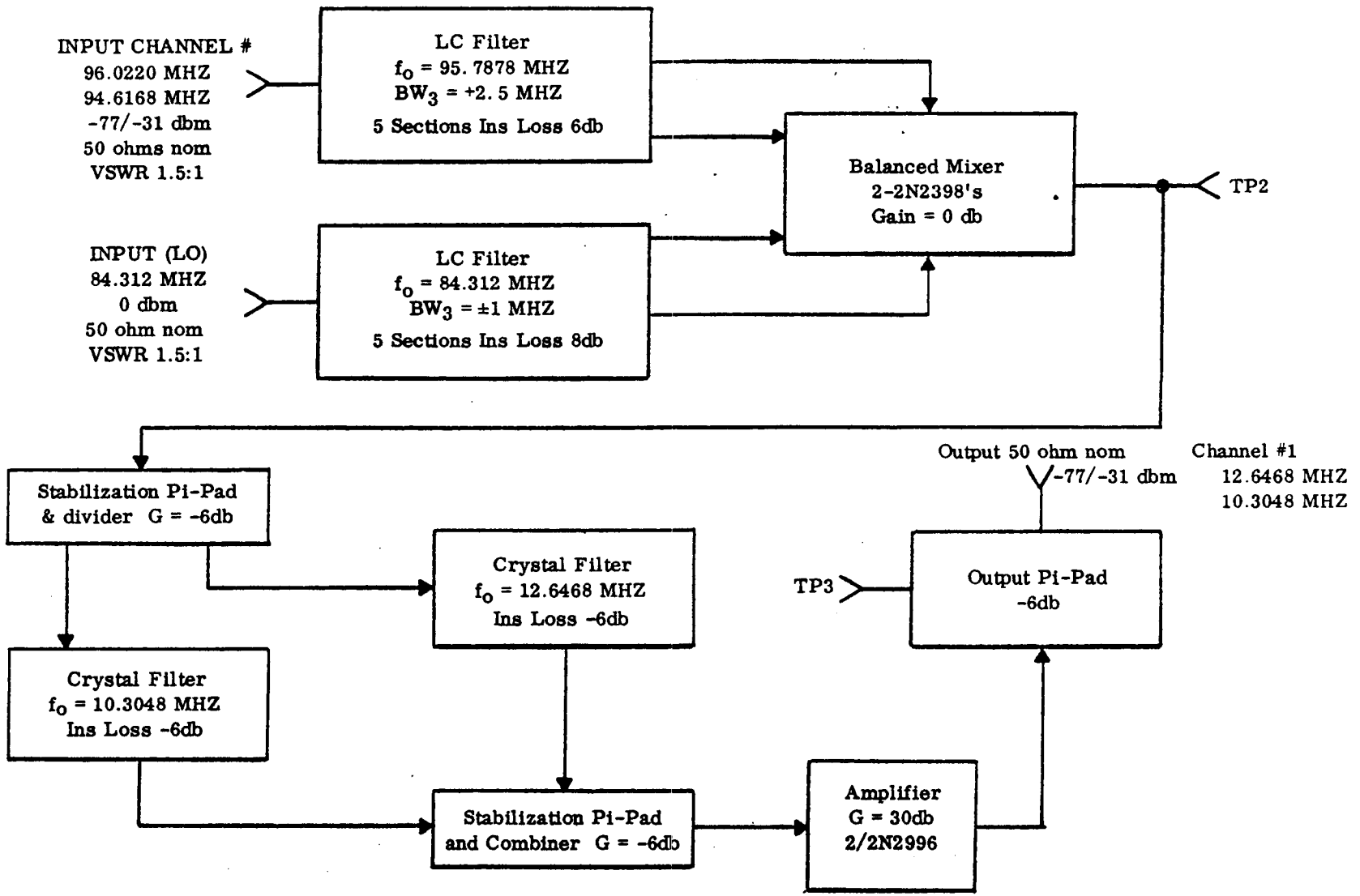


Figure 2-3. Block Diagram - 2nd Mixer and Filter Module, Channel No. 1

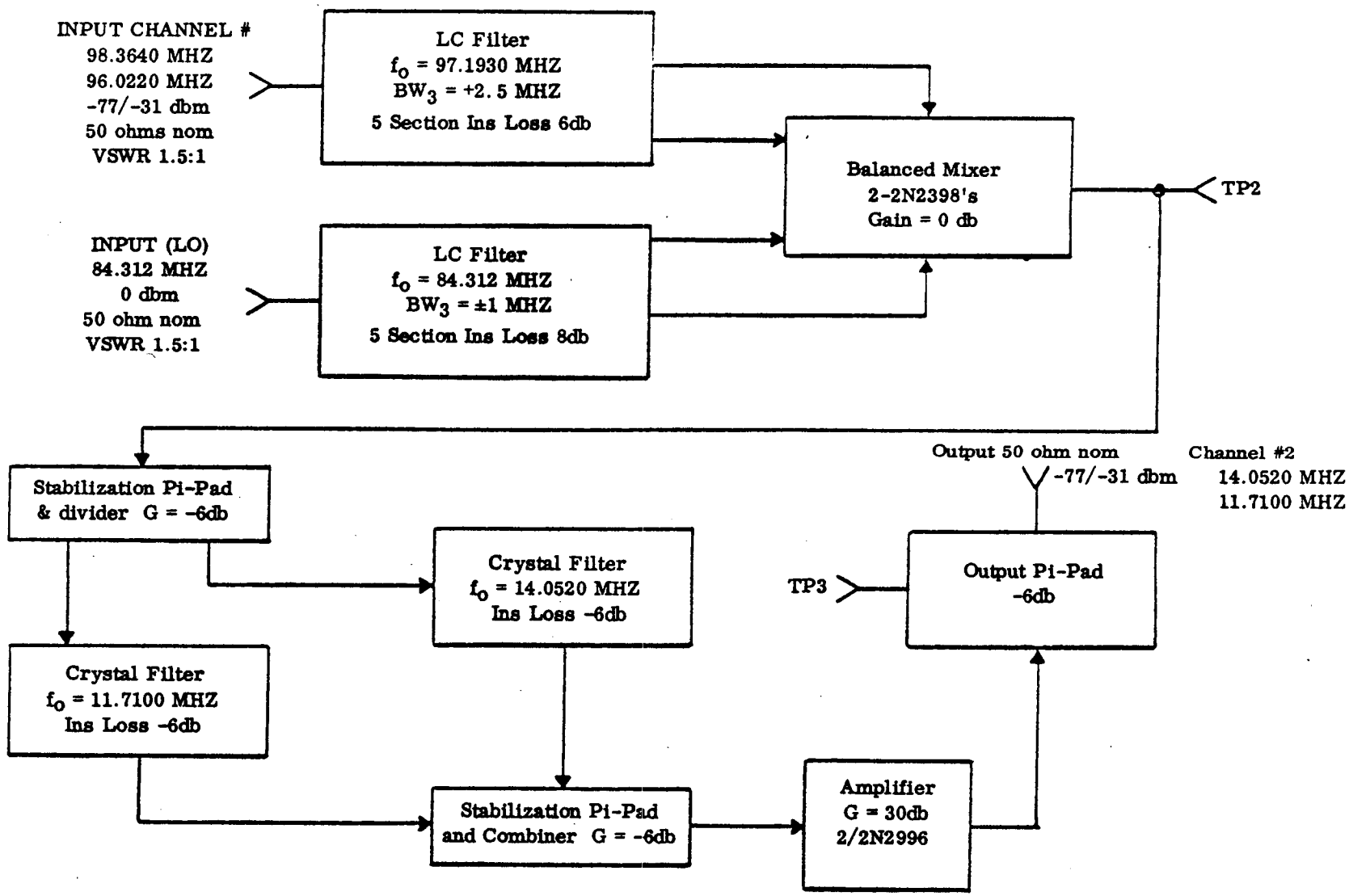


Figure 2-4. Block Diagram - 2nd Mixer and Filter Module, Channel No. 2

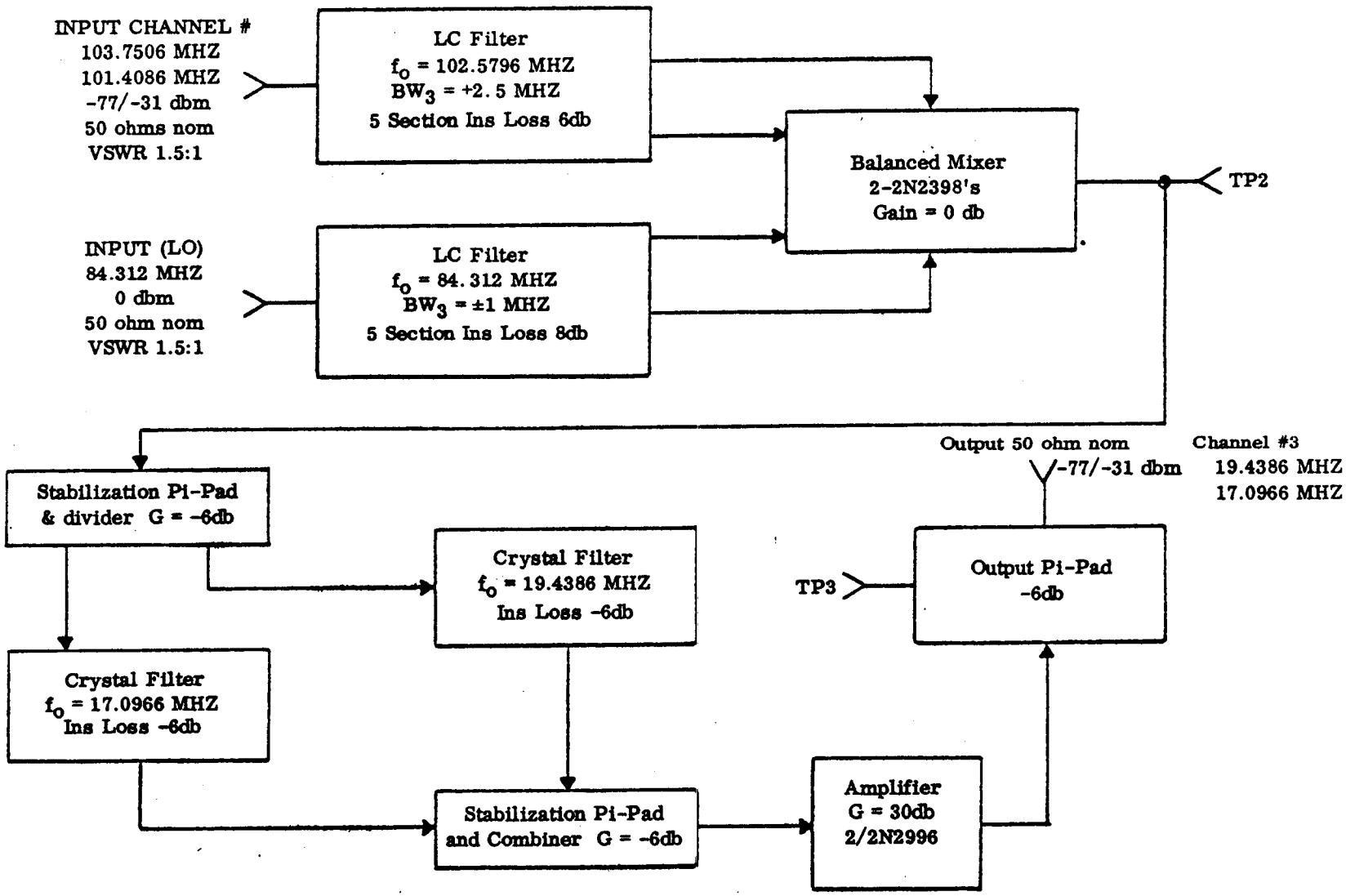


Figure 2-5. Block Diagram - 2nd Mixer and Filter Module, Channel No. 3

TABLE 2-3

SPECIFICATION FOR SECOND MIXER AND FILTER MODULE

1.	Input Frequency:	Channel 1 - 94.6168 MHz 96.9588 MHz Channel 2 - 96.0220 MHz 98.3640 MHz Channel 3 - 101.4086 MHz 103.7506 MHz Channel 4 - 102.8200 MHz 105.1558 MHz
2.	L.O. Input Frequency:	84.3120 MHz (All channels) Level 0 dbm
3.	Tuning Range:	Fixed for each channel
4.	Output Frequencies and Bandwidths (BW_3)	Channel 1 - 12.6468 MHz (20 KHz) 10.3048 MHz (200 KHz) Channel 2 - 14.0520 MHz (20 KHz) 11.7100 MHz (200 KHz) Channel 3 - 19.4386 MHz (20 KHz) 17.0966 MHz (200 KHz) Channel 4 - 20.8438 MHz (20 KHz) 18.5018 MHz (200 KHz)
5.	Noise Figure:	10 db Max. (Test run in conjunction with Module #2)
6.	Phase Characteristic:	Phase deviation with temperature not to exceed ±0.3 deg. at specified center frequency, 0° C to +60° C is design goal. (25° C ±10° C minimum) and phase deviation with temperature to match in channel pairs and = ±1% from Linear BW_3 design goal.
7.	Input/Output Impedance:	50 ohm Nom. VSWR 1.5:1 Max.
8.	Input/Output Connectors:	Microdot 31-50 or equivalent
9.	Gain: (Overall)	Unity gain ±2 db
10.	L.O. Isolation:	(IF output) 30 db minimum
11.	Dynamic Range:	No compression -77 dbm to -31 dbm
12.	Power Input:	-18 VDC @ 20 ma Connector DE9P
13.	Size: Weight:	2 3/4" high x 3 7/8" wide x 9 1/2" long 3 lbs.
14.	Temperature:	25° C ±10° C minimum 0° C to 60° C design goal

NOTE: Each channel input filter to be tuned for optimization of the desired signal.

The video amplifier output is also fed to a second video amplifier in order to increase the level before detection. The output of this video amplifier is fed to a diode detector. A 2.342 MHz amplifier and a transformer is used to provide 3 outputs at 2.342 MHz. A test point, TP-6, is provided ahead of the video detector. NOTE: On Channel 2, which was the first channel built, a two-stage video amplifier feeds the detector with no gain at 2.342 MHz following. This arrangement limits on high noise peaks (when receiving a weak signal) and prevents proper operation of the signal-to-noise detector in the P.L.L. Filter Module. This was changed to the above arrangement on Channels 1 and 3.

A DC voltage is also derived from the diode detector, which is proportioned to the uncorrelated signal level at the detector. This negative voltage is fed to a diode gate and to an AGC amplifier. Its level is adjustable by R-2. This voltage is well filtered. When lock-on to a signal is achieved, the correlated voltage from the correlation detector over-rides the uncorrelated detector voltage and locks it out of the circuit. The channel then operates on correlated AGC voltage.

The AGC system in this module consists of the diode gate whose output is fed to Q-12 a PNP Silicon 2N1036 Transistor. Potentiometer R-3 in the emitter circuit of Q-12 adjusts the AGC DC level, and hence the amplifier output level. The output of the 2N1036 is fed to a two-stage cascaded DC amplifier Q-11 and Q-10, both 2N336 transistors, which provides a 180 degree phase reversal. This amplifier in turn feeds two emitter follower drivers Q-9 and Q-8, 2N336 transistors, whose output DC range is controlled by diode CR-2. Another diode, CR-7, prevents the bases of Q-8 and Q-9 from going more than one-half volt negative. The two separate emitter followers feed the metering system and the AGC buss line to the tetrodes. A jumper is required on the power plug, P-2, between Pins 2 and 3 to close the AGC system. Removal of the jumper allows manual AGC operation during test by application of a 0 to +5 volt bias at Pin 3 of J-2.

All active circuitry is constructed on one printed board placed in the bottom of the module. Microdot printed board connectors (female) are used on the printed board for signal connections. A DE9P Cannon connector is used for power. The bandpass filter is placed on top of the chassis.

2.2.4 3rd I-F Converter Module

Refer to Figures 2-9, 2-10 and 2-11 for block diagrams of the 3rd I-F Converter Module. Refer to Table 2-5 for target specifications and to Figures 8-12, 8-13 and 8-14 for schematics of this module. The basic purpose of this module is to convert signals in the 12 to 21 MHz range to a signal at 4.684 MHz. It also produces the required L.O. signal from two reference signals. This module is a unity gain module

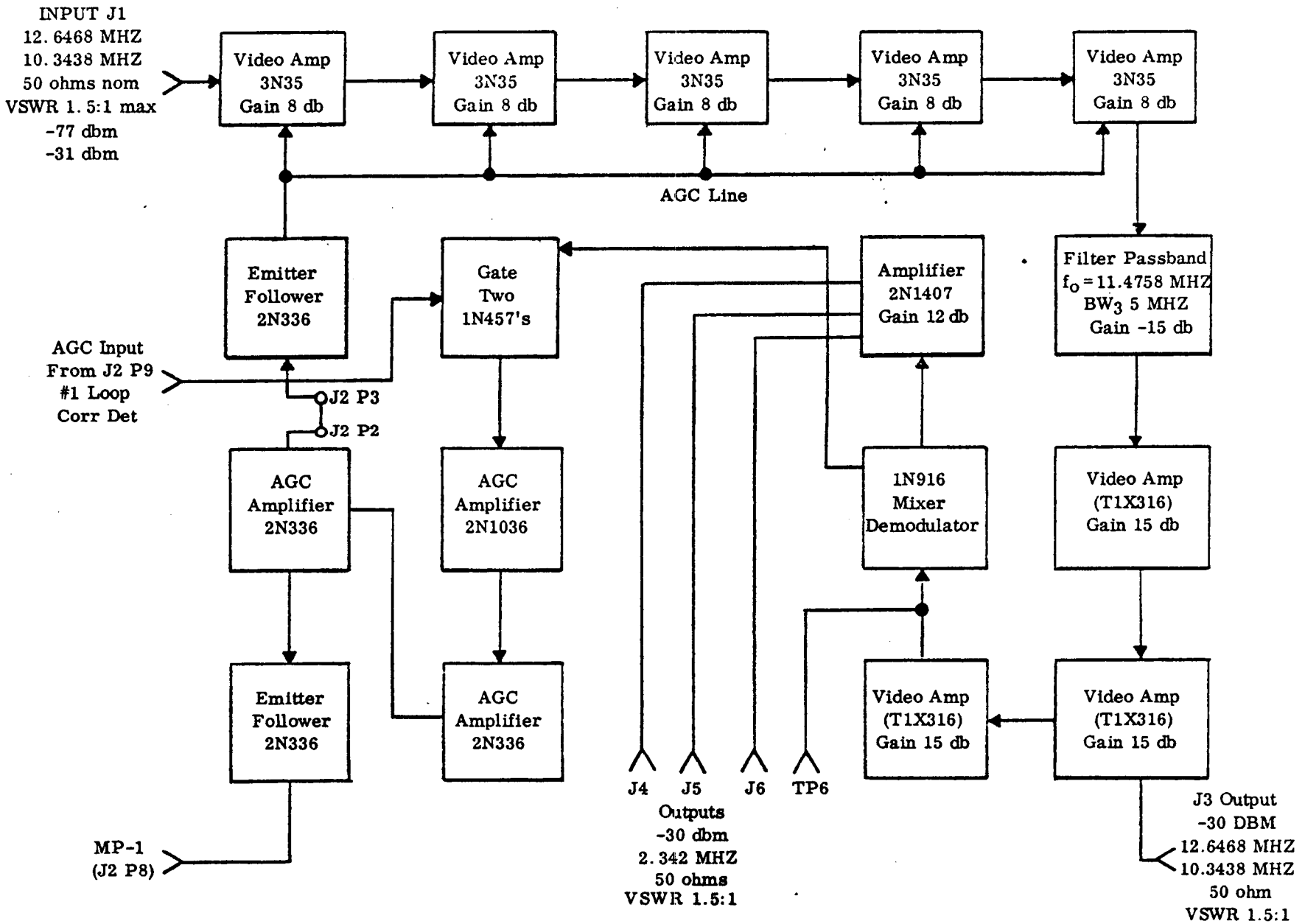


Figure 2-6. Block Diagram - 2nd IF Amplifier Module, Channel No. 1

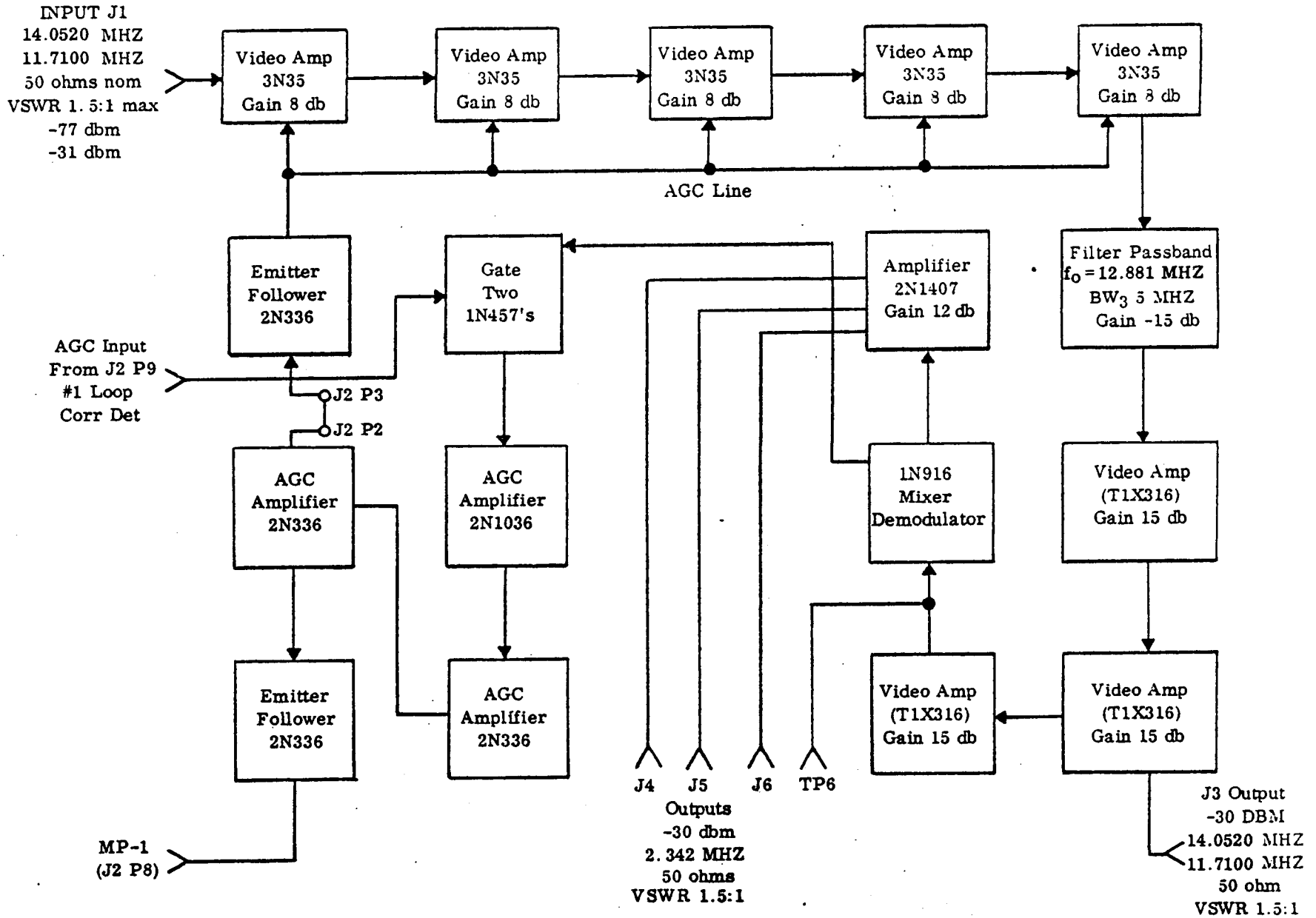


Figure 2-7. Block Diagram - 2nd IF Amplifier Module, Channel No. 2

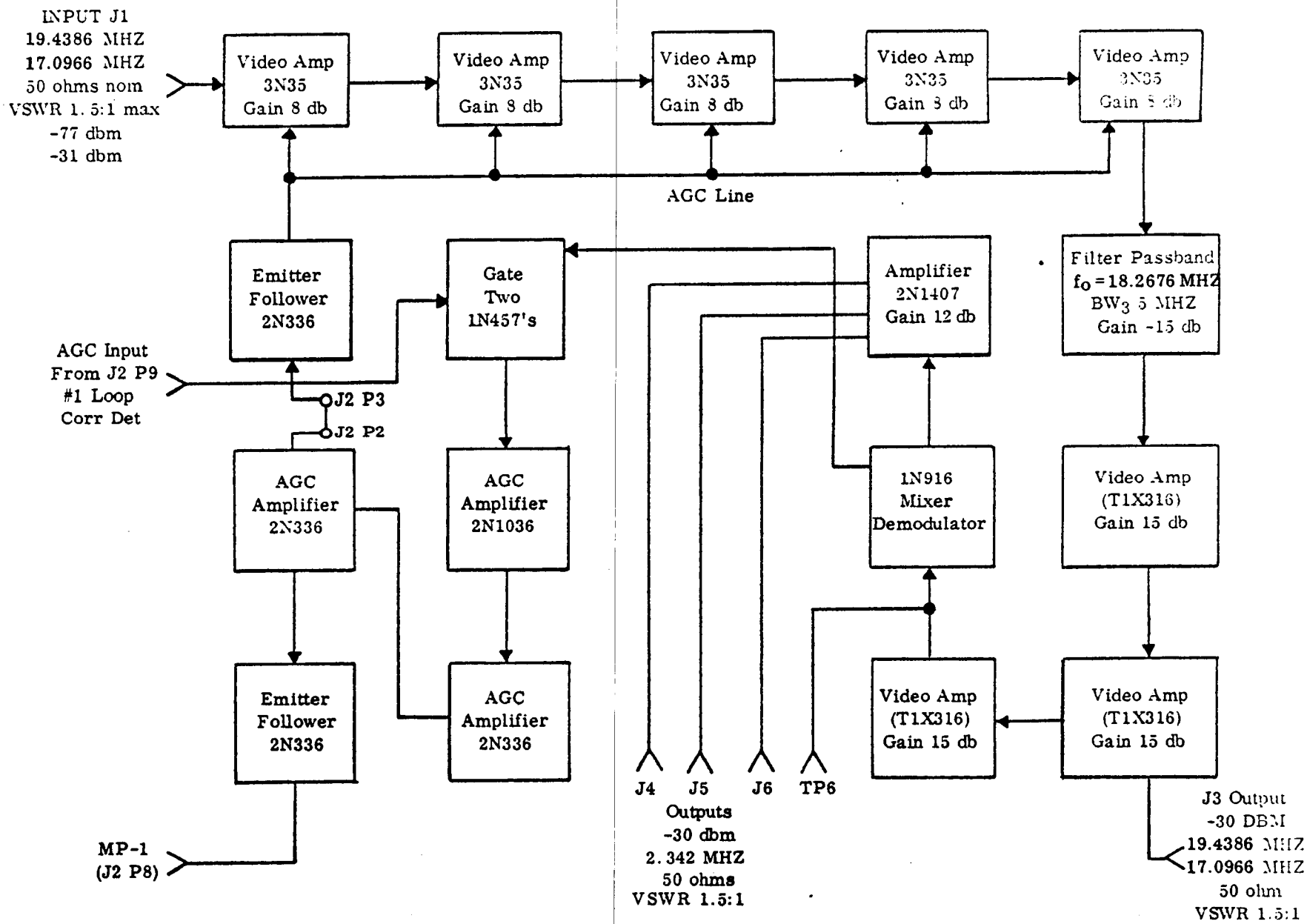


Figure 2-8. Block Diagram - 2nd IF Amplifier Module, Channel No. 3

TABLE 2-4

SPECIFICATION FOR SECOND I-F AMPLIFIER MODULE

1.	Input Frequency:	Channel 1 - 10.3048 and 12.6468 MHz Channel 2 - 11.710 and 14.052 MHz Channel 3 - 17.0966 and 19.4386 MHz Channel 4 - 18.5018 and 20.8438 MHz
2.	Input Level:	-77 dbm
3.	Gain:	60 db ±2 db
4.	AGC Control Range:	60 db minimum
5.	AGC Linearity:	(TBD)
6.	Output No. 1:	-17 dbm - Channel 1 - 10.3048 and 12.6468 MHz Channel 2 - 11.71 and 14.052 MHz Channel 3 - 17.0966 and 19.4386 MHz Channel 4 - 18.5018 and 20.8438 MHz
	Output No. 2:	0 dbm - Channel 1 - 10.3048 and 12.6468 MHz Channel 2 - 11.71 and 14.052 MHz Channel 3 - 17.0966 and 19.4386 MHz Channel 4 - 18.5018 and 20.8438 MHz
	Output Nos. 3, 4, 5:	0 dbm - 2.342 MHz (Detected output)
7.	AGC Loop Gain:	TBD
8.	ACG Input:	0 to -4 volts DC
9.	AGC Output:	0 to +4 volts DC
10.	Input/Output Impedance:	50 ohms nominal
11.	Input/Output VSWR:	1.5:1 maximum
12.	Noise Figure:	10 db maximum
13.	Bandwidth:	>15 Mc
14.	Phase Characteristic:	TBD
15.	Power Input:	+18 VDC @ 20 ma -18 VDC @ 20 ma DE9P Connector

TABLE 2-4 (Cont.)

16.	Size:	2 3/4" high x 3 7/8" wide x 9 1/2" long
	Weight:	2.5 lbs.
17.	Temperature:	25° C $\pm 10^{\circ}$ C minimum
		0° C to 60° C design goal

but high isolation of L.O. signals from the signal output is a necessity. Therefore, the module is made in two separated sections each of which has its own printed board with a full partition and finger stock between partitions. Each section is powered by different power supplies, one on the -18 volt supply and the other on the +18 volt power supply.

Each channel's block diagram shows the input frequencies and levels which are fed to J-2. These block diagrams also show the L.O. signals fed to J-4 and J-6 in each case. First let us consider the second section which is powered by the +18 volt supply. This section has a 4.684 MHz input from the synthesizer. It also has an output of this signal and only a very small amount of 4.684 MHz energy is actually used by this module. The output connector must be terminated in 50 ohms in order to load the 4.684 MHz input, which otherwise would not be properly matched. Section 2 also receives a second frequency from the synthesizer whose frequency varies from channel to channel but is always a coherent signal and is harmonically related in all cases. This second signal is attenuated by use of a 20 db pi pad to lower its level for isolation purposes.

Both signals are mixed in a transistor balanced mixer stage using two 2N2398's. A balancing potentiometer R-18 is provided to balacne out both input signals and leave only the sum and difference signals. A pi coupling network is used to couple only the difference frequency to a crystal filter. The crystal filter passes only the difference product and attenuates all other signals with the help of other selective devices by 100 db. The difference frequency (consult block diagram for channel frequency) is then amplified by a 2N2398 transistor stage and fed to output jack J-9.

NOTE: When module is in system operation a connector is placed between J-9 and J-3.

This completes Section 2 whose purpose is to develop a coherent L.O. signal from two synthesizer signals.

The first section of the 3rd I-F Converter Module converts a signal in the 12 to 21 MHz range, dependent on the channel in use to a 4.684 MHz signal. The gain will depend on the level of the reference signals supplied, and may be as high as 15 db. The signal to J-2 passes through a LC filter of 5% wide bandwidth and then to a balanced mixer. The output signal of Section 2 is fed to J-3 and from there to the balanced mixer. A potentiometer R-7 is provided to balance out the input signals leaving only the sum and difference signals at the mixer output. A pi coupling network couples the difference signal to a filter with a BW_3 of 1 MHz. Attenuation of undesired signals is 100 db or better with this combination. The filter output power is divided to two separate output amplifiers using 2N1566A with a dual pi coupling network. Each amplifier is coupled to

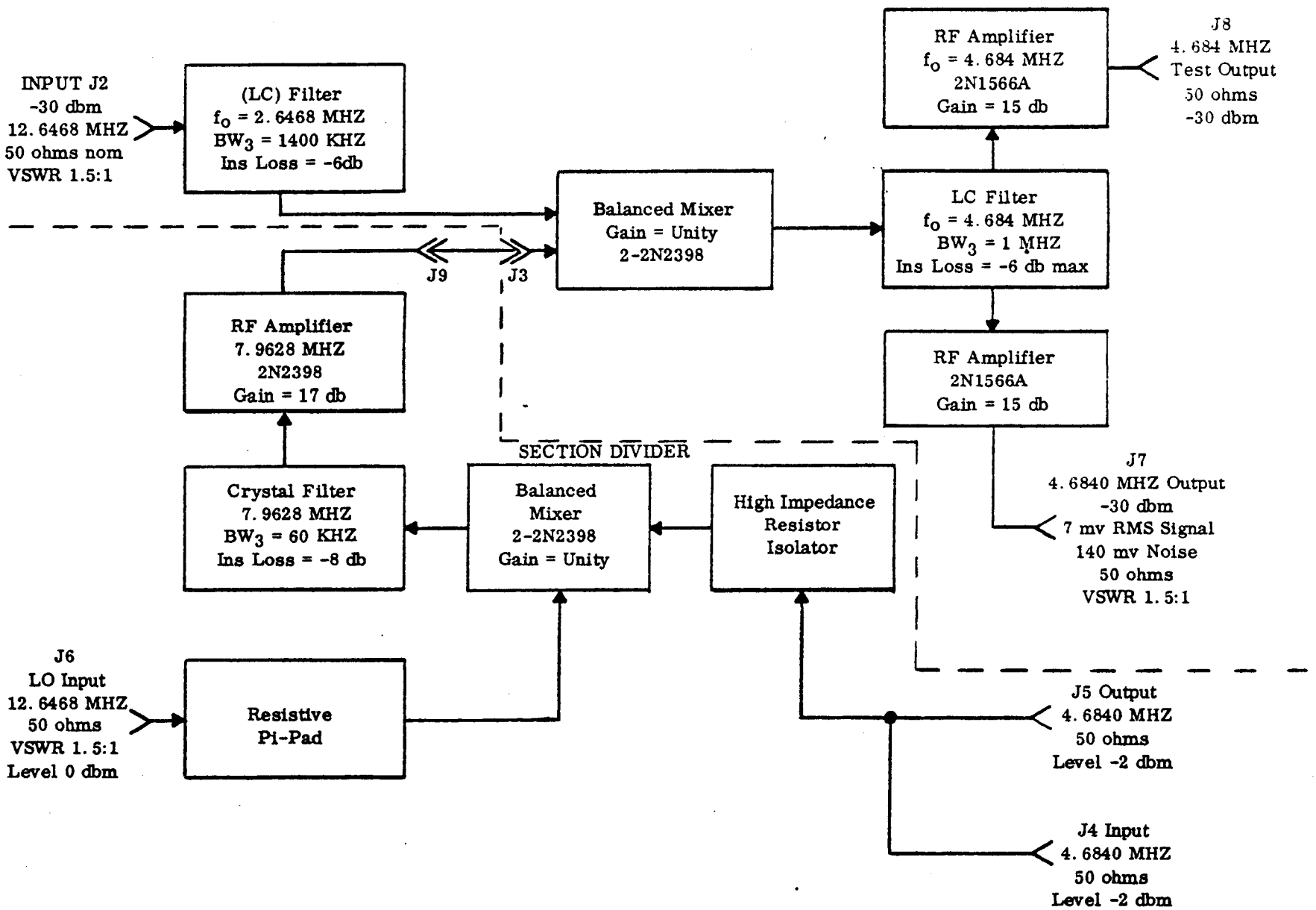


Figure 2-9. Block Diagram - 3rd IF Converter Module, Channel No. 1

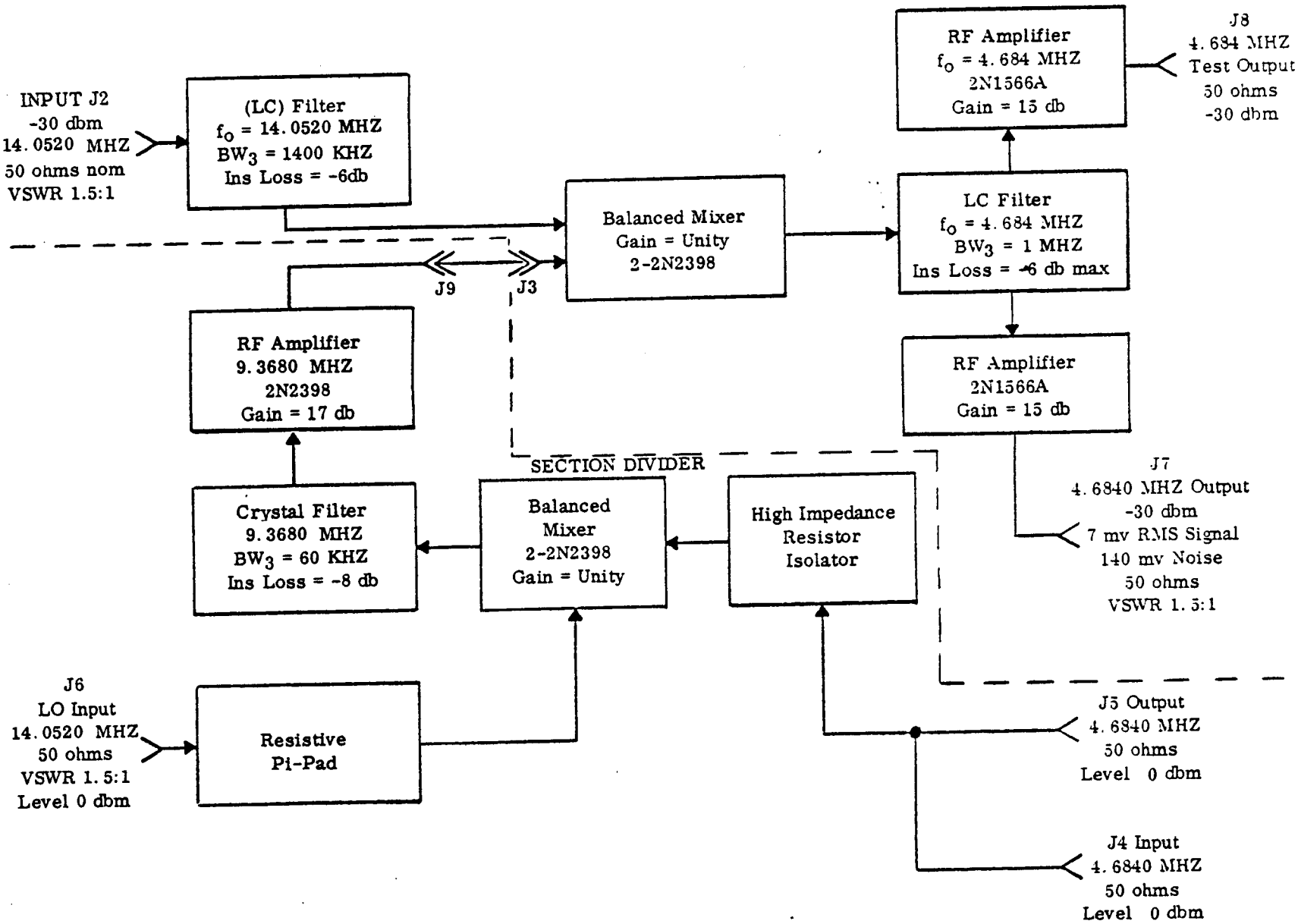


Figure 2-10. Block Diagram - 3rd IF Converter Module, Channel No. 2

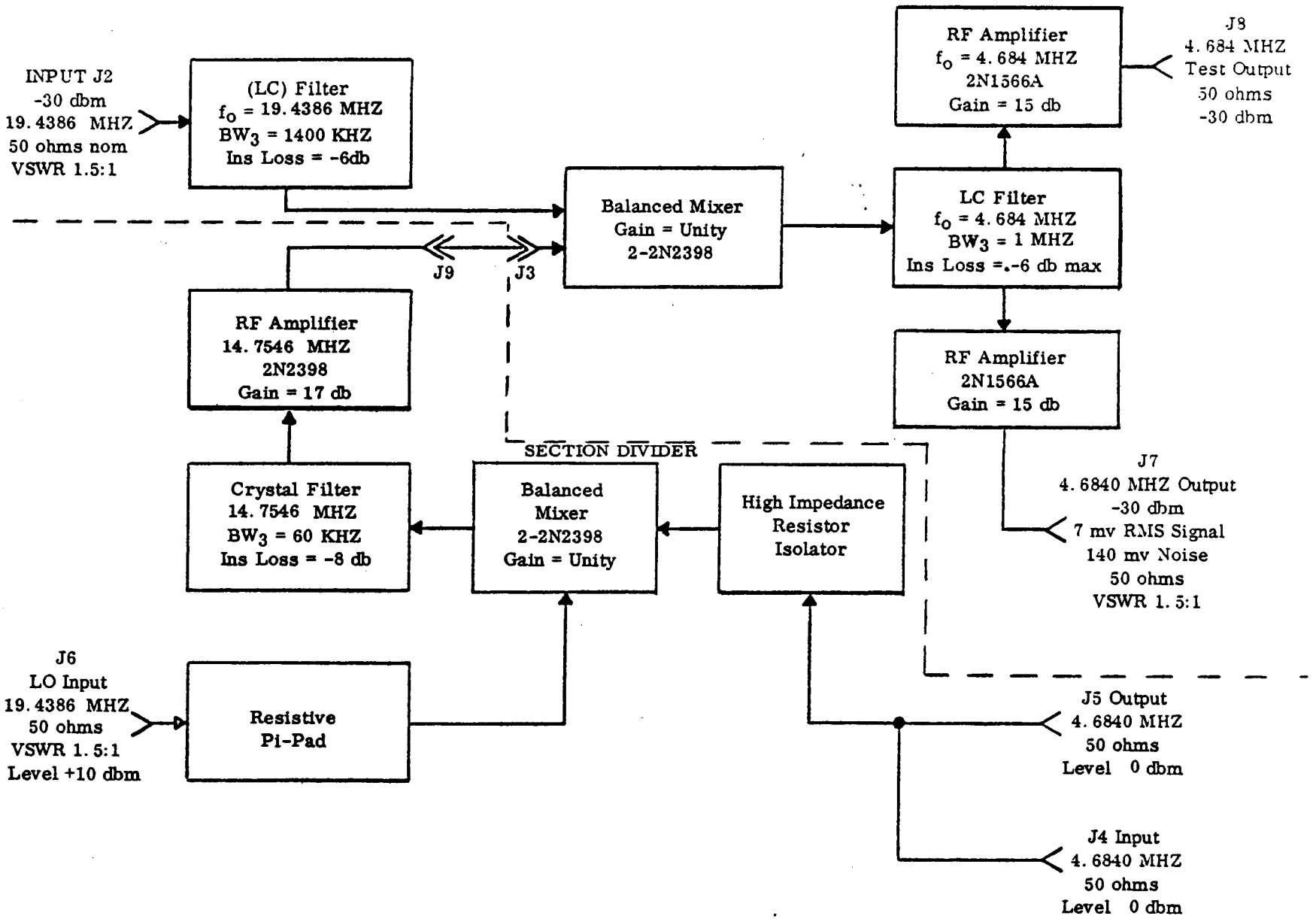


Figure 2-11. Block Diagram - 3rd IF Converter Module, Channel No. 3

TABLE 2-5

3RD I-F CONVERTER MODULE

1.	Input Frequency:	Channel 1 - 12.6468 MHz Channel 2 - 14.052 MHz Channel 3 - 19.4386 MHz Channel 4 - 20.8438 MHz
2.	Input Level:	-30 dbm
3.	Output Frequency:	4.684 MHz
4.	Output Level:	-30 dbm
5.	Gain:	Unity ±2 db (adjustable)
6.	Bandwidth:	Input - ±700 KH 2 (BW_3) Output - ±3 KC (BW_6)
7.	Reference Inputs:	4.684 MHz +10 dbm level 12.6468 MHz +10 dbm level - Channel 1 14.052 MHz +10 dbm level - Channel 2 19.4386 MHz +10 dbm level - Channel 3 20.8438 MHz +10 dbm level - Channel 4
8.	Reference Output:	4.684 MHz 0 dbm level
9.	RF Impedance:	50 ohm nominal
10.	RF VSWR:	1.5:1 maximum
11.	Phase Characteristic:	TBD
12.	Power Input:	+18 VDC @ 25 ma -18 VDC @ 25 ma DE9P Connector
13.	Size: Weight:	2 3/4" high x 3 7/8" wide x 9 1/2" long 3 lbs.
14.	Temperature:	25° C ±10° C minimum 0° C to 60° C design goal

an output connector using pi coupling networks to J-7 and J-8. J-7 is used for the signal output and J-8 for a test output. Both are the same level and all connectors are Microdot printed board female connectors at 50 ohm.

Each section is made on a separate printed board occupying one-half of the module with a shielding partition between the boards.

2.2.5 4.684 MHz Phase Detector Module

Refer to Figure 2-12 for a block diagram of the 4.684 MHz Phase Detector Module. Refer to Table 2-6 for target specifications and to Figure 8-15 for a schematic of this module. This module is designed to provide both a phase and a correlation output. The phase detected output is used in the #1 phase-lock loop to synchronize the VCO. The correlation output is provided by a similar detector in which the reference voltage is phase shifted 90 degrees.

Separate single stage amplifiers are used on each input to each detector to provide the required level and sufficient isolation between detectors. As can be seen in the schematic of Figure 8-15 the detectors are constructed with matched pairs of diode quads. The reference signal to each quad is tailored to provide a DC balance to within less than 2 millivolts.

The phase detector output is provided at a level of 0.25 volt per radian with rated 7 to 10 millivolt input signal. A dynamic range of about 26 db is provided to hold intermodulation and noise to a minimum.

The correlation detector is identical to the phase detector except for the reference phasing.

The correlation detector output at TP-1 is approximately -0.25 volts. A low pass RC filter with a 20 Hz break frequency is used to reduce noise peaks that could overload the amplifier which follows. This amplifier consists of a P65A Philbrick differential amplifier with feedback adjusted to provide a gain of approximately 16.

The resulting amplified correlation outputs are provided for AGC, for acquisition circuits and for the correlation meter.

2.2.6 PLL Filter Module

This module performs the following functions:

a. PLL filter for 4.684 MHz phase-lock loop.

b. Acquisition for 4.684 MHz phase-lock loop.

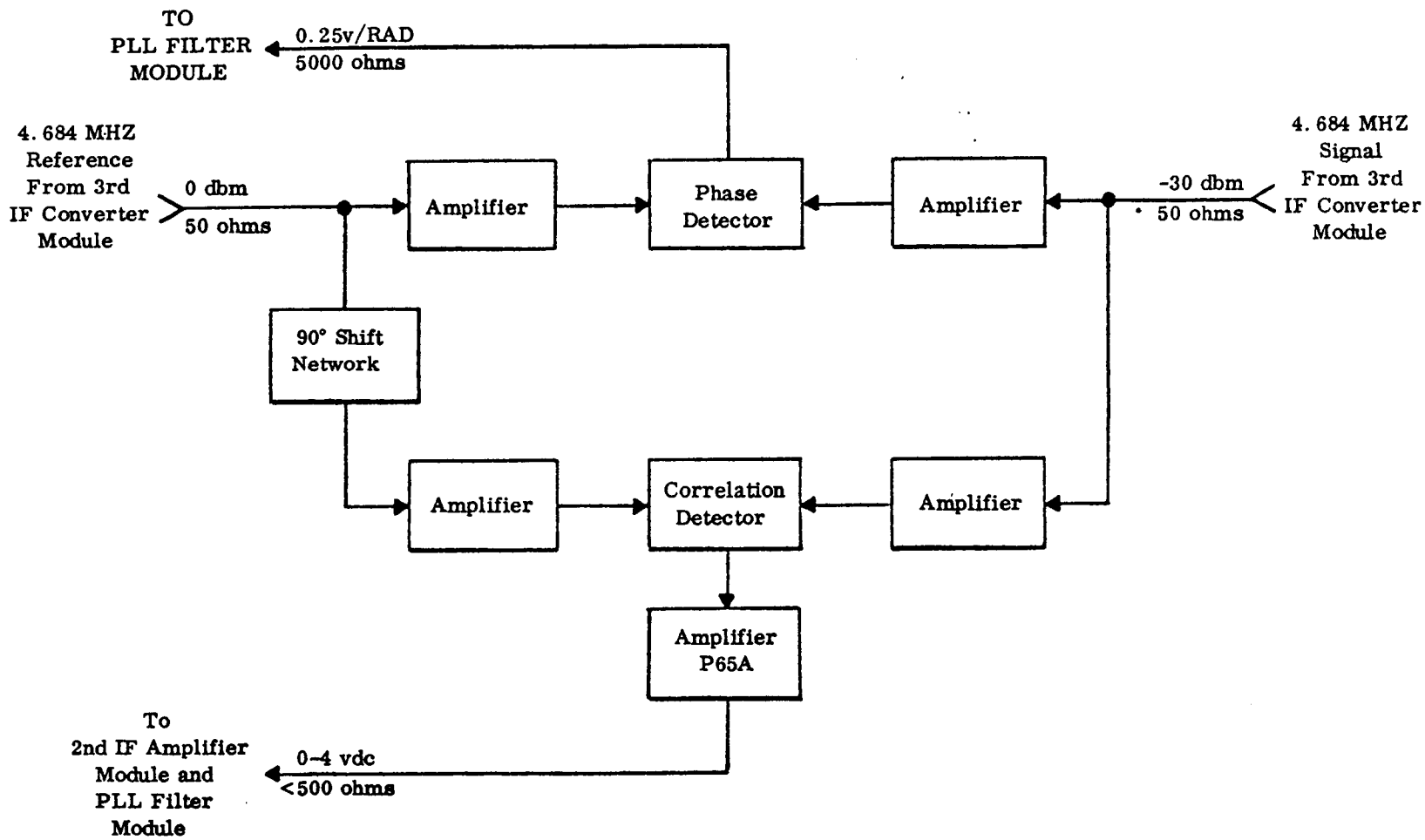


Figure 2-12. Block Diagram - 4 684 MHZ Phase Detector Module

TABLE 2-6

SPECIFICATION FOR 4.684 MHz PHASE DETECTOR MODULE

1.	Inputs:	Signal Input J-2:	Frequency 4.684 MHz Power -30 dbm Impedance 50 ohm
		Reference Input J-1:	Frequency 4.684 MHz Power 0 dbm Impedance 50 ohm
2.	Outputs:	Correlation Detector: J3-9	Voltage 0 to -4 V Impedance 500 ohm BW 15 cps
		Phase Detector: J3-8 (Gnd. Return J3-7)	0.25 V/RAD phase error Impedance 5000 ohm
		Correlation Signal: J3-6	Level 0 to -4 V.
		Correlation Meter: Current J3-3	As required for Front Panel Meter
3.	Power Input:		+18 VDC @ 42 ma -18 VDC @ 42 ma DE9P Connector
4.	Size:		2 3/4" high x 3 7/8" wide x 9 1/2" long
	Weight:		3.2 lbs.
5.	Temperature:		25° C ±10° C minimum 0° C to 60° C

c. Acquisition for 2.342 MHz phase-lock loop.

d. Signal-to-noise ratio indicator circuits.

Refer to Figure 2-13 for a block diagram of the PLL Filter Module. Refer to Tabel 2-7 for target specifications and to Figure 8-16 for schematic.

The phase-lock loop filter for the #1 loop uses a passive and an active section. The passive section consists of R-43, R-44 and C-28. The input to this section comes directly from the 4.684 MHz phase detector in Module #3. The output of this filter goes to the positive input of A-1 a Philbrick Model PP65A operational amplifier in the active filter.

The active filter consists of a differential amplifier A-1, a capacitor C-26, and resistor R-45. The output of this filter section goes through R-81 directly to the 10.539 MHz VCXO in the VCO-1 module.

A low-pass filter with a relatively high break frequency is formed by R-81, C-32 and C-30. The break of this filter is high enough that it is essentially out of the circuit so far as the loop filter is concerned. However, it is effective in reducing the tendancy for the loop to lock onto artificially generated side bands. As can be noted, C-30 is in parallel with C-32 prior to acquisition when relay K-1 is not energized. Upon acquisition K-1 opens the ground return to C-30 thus reducing this filter to R-81 and C-32 only.

The lower break frequency is required prior to lock on because of the much greater loop gain in the phase-lock loop due to AGC level.

A tuning circuit is employed to maintain the proper charge on the loop filter capacitors prior to signal acquisition and lock on. This tuning loop consists of a differential amplifier, A-2, and its associated resistors, R-80, R-79, R-65 and a capacitor, C-31. A tuning voltage level, near zero for center frequency, is selected by R-67. This voltage is compared by means of the differential inputs to A-2, and the difference is used to provide current through R-65 and contacts of K-1 to charge C-28. This charge in turn causes the charge on C-26 to be corrected through amplifier A-1 and thus maintain the output to VCXO-1 equal to the value set-up by R-67. Upon acquisition K-1 is energized thus breaking the tuning loop and allowing the phase detector and the phase-lock loop to take over with the minimum voltage transient.

A double emitter follower consisting of Q-11 and Q-12 is used to provide a low impedance output for Doppler Polarity Indication which is also isolated sufficiently from the phase-lock loop.

The double emitter follower consists of an NPN followed by a PNP transistor. These transistors are carefully matched to maintain a nearly equal and opposite base to emitter potential difference. The output zero voltage crossing is within 0.1 volts of the input which is the VCXO control voltage.

A frequency analog voltage is provided from the output of Q-12 by a three resistor adding network consisting of R-62, R-63 and R-78. This voltage known as MP-1 varies from zero to about +5 volts. The output impedance of this circuit is less than 5 thousand ohms.

The acquisition circuit for loop #1 is represented by stages Q8 through Q10. The correlation detector provides an input to Q8 which inverts the signal and turns on relay driver Q9. The relay K-1 closes and turns on the front panel acquisition lamp and also removes the tuning voltage from the PLL filter. Q10 provides the logic signal output to the command circuits, zero volts when unacquired and +5 when acquired.

Q13 and Q14 comprise the acquisition circuitry for phase-lock loop #2. The correlation detector signal is inverted in Q13 and turn on the relay driver Q14. The relay is located in the VCO-2 module and is used to modify the filter circuits in the second loop as well as disconnection of the tuning voltage.

The signal-to-noise indicator circuit is designed to amplify the noise existing in a portion of the passband of the 2.342 MHz output of the 2nd I-F Amplifier Module and to use it to trigger a pre-set switch to indicate that the noise has risen above the pre-set threshold. The noise spectrum is selected and narrowed by the 2.305 MHz bandpass filter and is amplified by stage Q1 and Q2. The noise is rectified by CR-2 to provide a DC analog noise level voltage. Since the signal level is held constant due to correlation AGC, this analog noise level is also inversely proportional to the signal-to-noise ratio. Hence the analog output can be calibrated in terms of signal-to-noise ratio. An emitter follower Q3 delivers this voltage to MP3 for telemetering.

The analog noise signal is also applied to the base of a transistor, Q4, whose emitter voltage level is adjustable. Thus, the signal level at which Q4 conducts can be varied. When Q4 conducts, its collector voltage becomes less positive, triggering the Schmitt trigger composed of Q5 and Q6. The output of the Schmitt trigger drives the base of Q7, which when not conducting allows its collector which is the S/N indicator output to rise up to a 4 volt potential. When Q7 conducts and is saturated, its collector is about 0.2 volts above ground. Thus the two desired states of zero or +5 volts is produced.

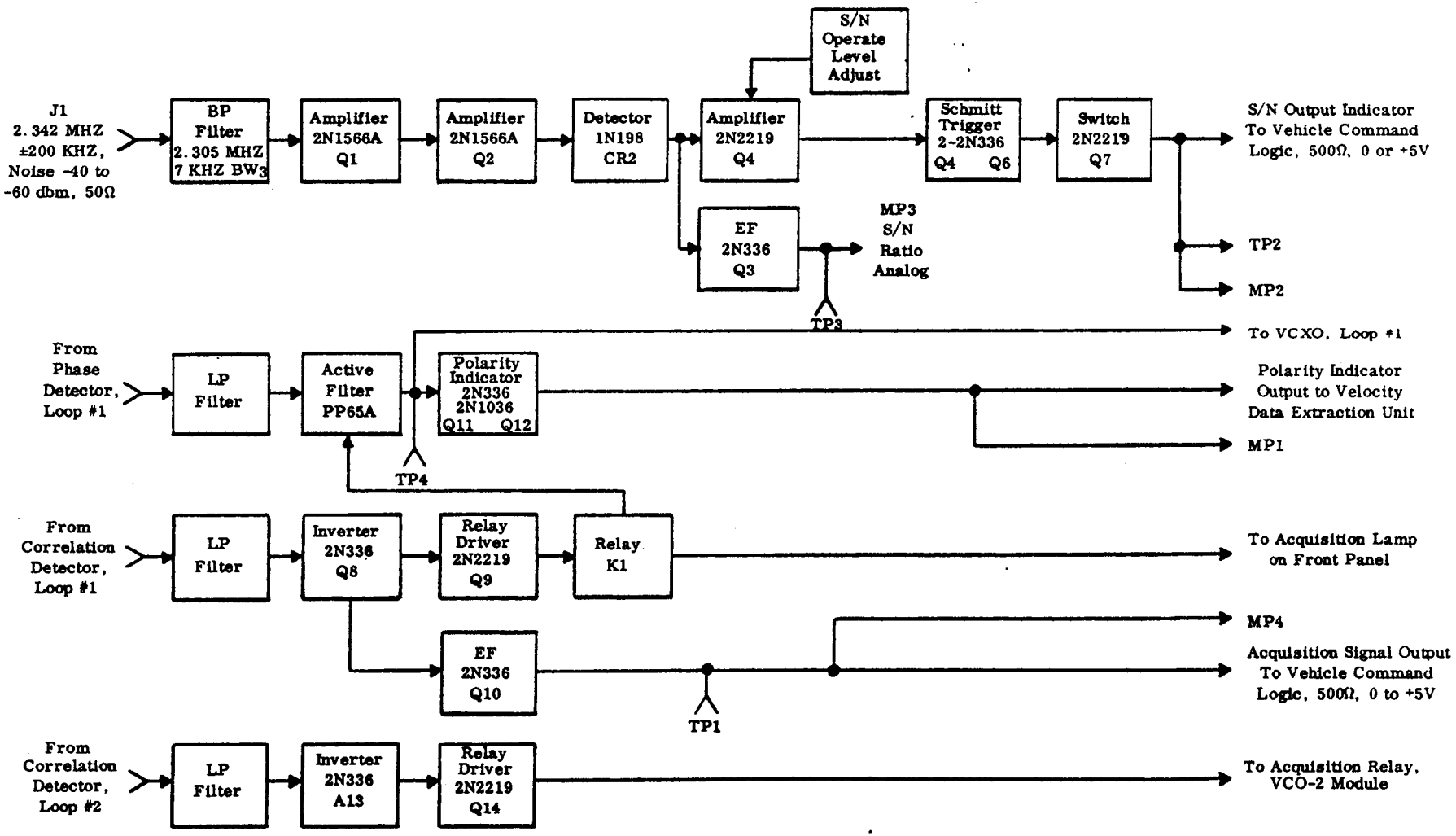


Figure 2-13. Block Diagram - Phase Lock Loop Filter Module

TABLE 2-7

SPECIFICATION FOR PLL FILTER MODULE

1.	PLL Filter and Polarity Indicator	
	a. Channel Input:	0.25 volts per radian from the Loop #1 Phase Detector
	b. Input and Output Connector:	DB-25P (Module Power Connector
	c. PLL Filter Channel Output:	+9 to -9 volts DC
	d. Polarity Indicator Output:	+9 to -9 volts DC depending on VCXO excursion above or below center frequency. Center frequency output 0 ±0.1 V.
	e. Output Impedance:	1000 ohms or less from polarity indicator
	f. Monitor Point:	MP1 - polarity indicator output (which is a measure of VCXO input signal)
	g. Test Point:	TP4 - VCXO input
2.	Signal-to-Noise Detector	
	a. Signal-to-Noise Channel Input:	Spectrum of signals and noise approximately 0 to 3 Mc in width, signal level -30 dbm, noise bandwidth 400 Kc, center frequency 2.305 MHz.
	b. Input Impedance:	50 ohms
	c. Filter Bandwidth:	7 KHz
	d. Input Connector:	Microdot 31-50 female
	e. Signal-to-Noise Channel Output:	Less than 0.2 volts DC when input signal-to-noise level is higher than a preset value which corresponds to signal-to-noise ratios in the main PLL bandwidth greater than 30 to 10 db ±5 ±10% volts DC when input signal-to-noise level is less than the preset value. Accuracy ±2 db.
	f. Output Impedance:	500 ohms

TABLE 2-7 (Cont.)

g.	Output Connector:	DB-25P (module power connector)
h.	Monitor Point:	MP-2 signal-to-noise ratio indicator output MP-3 signal-to-noise detector analog output All monitor points are positive DC output in the range 0 to 5 volts. Monitor point outputs are part of power connector (DB-25P)
i.	Test Points:	TP2 signal-to-noise ratio indicator output TP3 signal-to-noise detector input

3. Acquisition Channel, Loop #1

a.	Acquisition Channel Input:	0 to -4 volts DC
b.	Input and Output Connector:	DB-25P (module power connector)
c.	Input Impedance:	<500 ohms
d.	Acquisition Channel Output:	+0.2 volts DC or less when fine range loop is unlocked; +5 ±10% volts DC when fine range loop is locked. Additional output for acquisition lamp circuit closure
e.	Output Impedance:	500 ohms
f.	Test Points:	TP1 acquisition signal output, Loop #1

4. Acquisition Channel, Loop #2

a.	Acquisition Channel Input:	0 to -4 volts DC
b.	Input and Output Connector:	DB-25P (module power connector)
c.	Input Impedance:	<500 ohms
d.	Channel Output:	Driving signal to close the acquisition relay in VCO-2 Module. (Collector of NPN transistor with emitter at ground potential.)

TABLE 2-7 (Cont.)

5.	Power Input:	+18 VDC @ 120 ma +18 VDC @ 10 ma DE9P Connector
6.	Size: Weight:	2 3/4" high x 3 7/8" wide x 9 1/2" long 3.5 lbs.
7.	Temperature:	25° C ±10° C minimum 0° C to 60° C design goal

2.2.7 Voltage Controlled Oscillator VCO-1

Figure 2-14 is a block diagram of the VCO-1 Module. Refer to Table 2-8 for target specifications and to Figure 8-17 for a schematic of this module.

The Damon voltage controlled crystal oscillator, VCXO, is centered at 10.539 MHz with 0 V control on the input. The frequency of the VCXO varies 2.2 KHz per volt with positive and negative changes in control voltage. The 0 dbm, 50 ohm output from the VCXO is coupled with an L matching network to the base of a times two transistor multiplier stage. The 21.078 MHz output from the doubler is connected directly to a times four multiplier which completes the times eight multiplication necessary. The required 84.312 MHz output from the quadrupler is coupled to an amplifier which provides gain and selectivity (rejection for harmonic modes). The output of this amplifier is coupled through a power divider which supplies inputs to two isolation amplifiers. The two output amplifiers supply 0 dbm, 50 ohm outputs at 84.312 MHz ±160 KHz. Neutralization of the output amplifiers and the power divider contribute to isolating the two outputs from one another by 40 db.

2.2.8 Doppler Detector Module

Figure 2-15 is a block diagram of the Doppler Detector Module. Refer to Tabel 2-9 for specifications and to Figure 8-18 for a schematic of this module.

The doppler detector module is required to provide an output signal from 2.5 Hz to 1.6 MHz (3 db points) at 10 mw into a 50 ohm load. Its inputs are 70.26 MHz and 140.52 MHz at 10 mw and 84.312 MHz at 1 mw. It is further required to provide outputs of 70.26 MHz and 140.52 MHz at 10 mw into 50 ohms. All input frequencies are fixed except the 84.312 MHz which will vary by not more than ±160 KHz depending upon a received doppler. A high degree of isolation is required between the 84.312 MHz input and the 70.26 MHz and 140.52 MHz inputs and outputs.

2.2.8.1 Input Filters

Two section bandpass filters are employed at each of the three inputs. These are designed to provide a 3 db bandwidth of the order of 5 to 6 MHz for the 84.312 MHz and the 140.52 MHz filters and about 3 MHz for the 70.26 MHz filter. Coupling between the input and output section of these filters is provided in part by the stray capacity between the piston capacitors used for tuning and is adjusted to approximately critical coupling by means of C3, C20 and C22. These capacitors consist of small metal tabs soldered to the tops of the piston capacitors. Adjustment is achieved by bending the tabs.

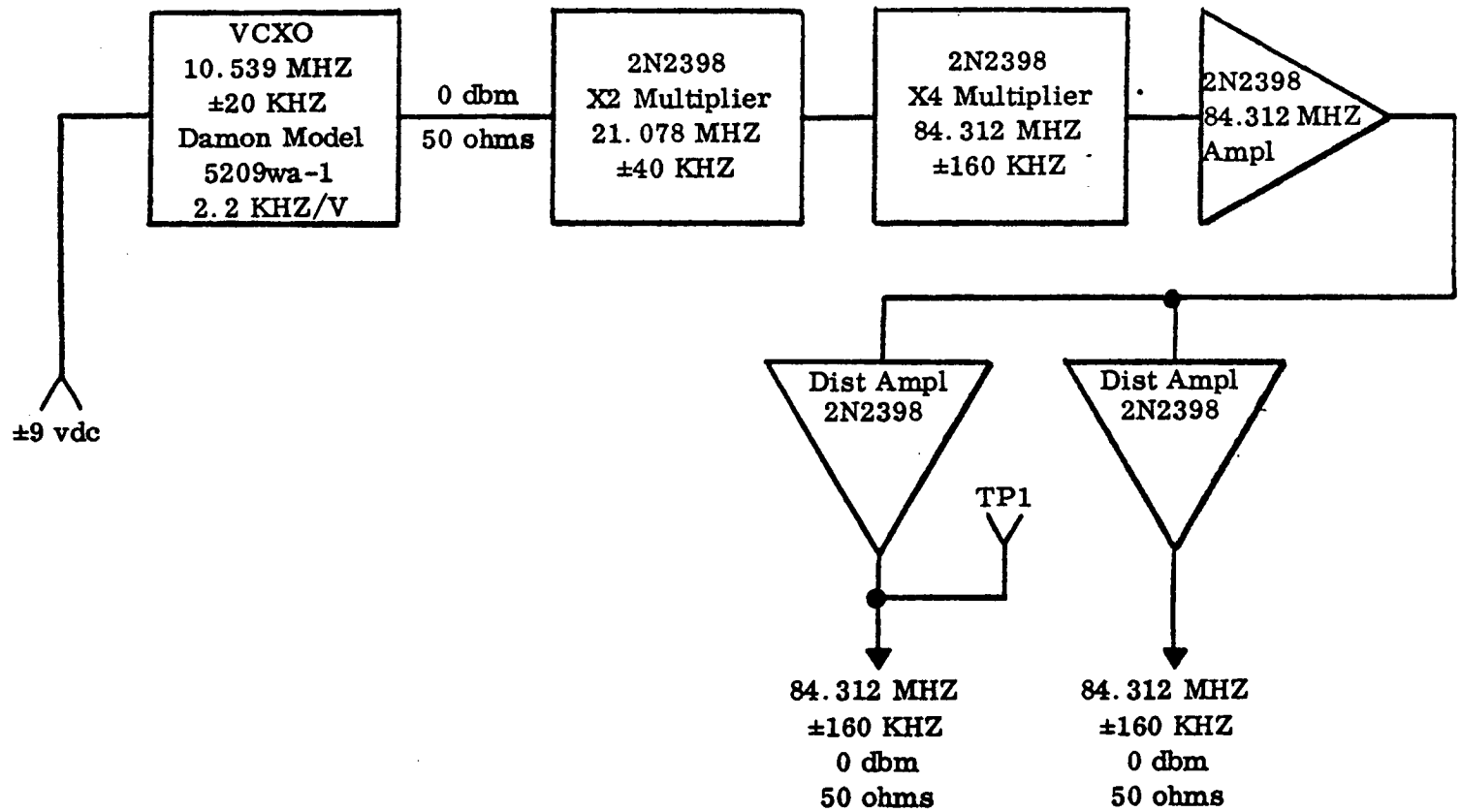


Figure 2-14. Block Diagram - VCO-1 Module

TABLE 2-8

SPECIFICATION FOR VOLTAGE CONTROLLED OSCILLATOR - VCO-1 MODULE

1.	Inputs:	DC Control Voltage ±9 V Input Impedance 720 K ohms
2.	Outputs:	Frequency: 84.312 MHz ±160 KHz Impedance: 50 ohms Power: 0 dbm
3.	Two outputs isolated by at least 40 db	
4.	Frequency Stability:	Short Term: 1.0 part in 10^8/50 msec Long Term: ±250 cps/yr
5.	Harmonic Suppression:	Not less than 40 db
6.	Power Input:	+18 VDC @ 30 ma DE9P Connector
7.	Size: Weight:	2 3/4" high x 3 7/8" wide x 9 1/2" long 2.70 lbs.
8.	Temperature:	25° C ±10° C minimum 0° C to 60° C design goal

The principal function of the input filters is to provide isolation between inputs, although they also serve to remove spurious signals which may be present on the input signals. It will be noted that two 1.2 K resistors are connected between the filter input and the module input jack for the 70.26 and 140.52 MHz inputs. These are used to provide further isolation and to prevent the filter from absorbing any significant amount of power from the input. Two resistors are used in series since at these frequencies the capacity reactance of the 1/4 W resistors will be relatively low.

2.2.8.2 High Frequency Mixer

A 2N2398, Q5, is used in the high frequency mixer. The 84.312 MHz signal is applied to the emitter and the 70.26 MHz signal to the base. This configuration was selected since it was felt that this would provide the maximum isolation of the 84.312 MHz (the variable frequency) from the 70.26 MHz input line.

The output circuit of this mixer is tuned to 14.052 MHz and matched to the next stage by a single pi section.

2.2.8.3 Multiplier Stages

The multiplier stages, Q6 and Q7, are quite conventional. They also employ 2N2398 transistors in a common emitter configuration. Q6 multiplies the 14.052 MHz by two providing 28.104 MHz. This is multiplied by five in Q7 providing 140.52 MHz. The interchange network following each mixer is a bandpass circuit with series capacitance match to the next transistor input.

2.2.8.4 Amplifier Stages

Two 140.52 MHz amplifier stages are employed, Q8 following the 5X multiplier and Q1 following the 140.52 MHz input filter. These are conventional common emitter stages. Q8 is biased for approximately maximum gain since its output may be considered as the local oscillator signal driving the emitter of the low frequency mixer Q2. The gain of Q1 is controlled by adjusting R34, a 50 K potentiometer in series with a fixed emitter resistor. This potentiometer is adjusted to provide the desired doppler output level.

2.2.8.5 Low Frequency Mixer

The low frequency mixer A2 is also a 2N2398. As mentioned above the emitter of this transistor is driven with 140.52 ±1.6 MHz from Q8. This is a relatively high level signal (about 400 mv) and because of the bandpass characteristics of the filters in the multipliers and the fact

that some of these stages are operating near saturation, the amplitude of this drive changes only slightly over the ±1.6 MHz frequency range. Thus the output of the mixer is nearly constant over this range. It should be noted that the only bias on this mixer is derived from this signal, and to a lesser degree from the 140.52 MHz fixed frequency applied to the base from A1. With no input signals this transistor is cut off.

The output load for this mixer is the 3.3 K collector resistor which also serves as the input termination of the low pass filter.

2.2.8.6 Low Pass Filter

A single pi section low pass filter is used between the low frequency mixer and the output emitter follower. This filter is designed with a cut-off frequency of about 2.2 MHz, and an input and output impedance of about 3000 ohms. A trap consisting of C12 and L6 is connected across the input of the filter and is tuned to 140.52 MHz The output of the filter is a-c coupled to the output emitter follower.

2.2.8.7 Output Emitter Follower

A cascade emitter follower employing two 2N2219 transistors is employed. Two transistors are used in order to provide a high input impedance and a low output impedance for driving the 50 ohm load. The coupling capacitor C15 is selected to have a 3 db low frequency cut-off of approximately 2.5 Hz when coupling the 3 K source to the 3K load.

The potentiometer, R11, serves as a zero adjustment to provide a d-c of zero volts at the emitter follower output. The collector voltage for the emitter followers is supplied from a 6.8 volt zener diode, CR1. This is done to reduce the dissipation of the output transistor which might be somewhat high at high ambient temperatures if the full 18 volt supply potential was used. A 36 ohm resistor, R12, is used between the output emitter and the output jack J6 in order to assure a VSWR of less than 1.5, since the output impedance of the emitter follower stage itself is only about 3.5 ohms.

2.2.9 VCO-2 Module

Figure 2-16 is a block diagram of the VCO-2 module. Refer to Table 2-10 for target specifications and to Figure 8-19 for a schematic of this module.

The VCO-2 module contains the phase-lock loop filter and the VCXO for the #2 or 2.342 MHz loop. The VCXO output is amplified by two parallel stages Q1 and Q2. One output is for the 2.342 MHz reference

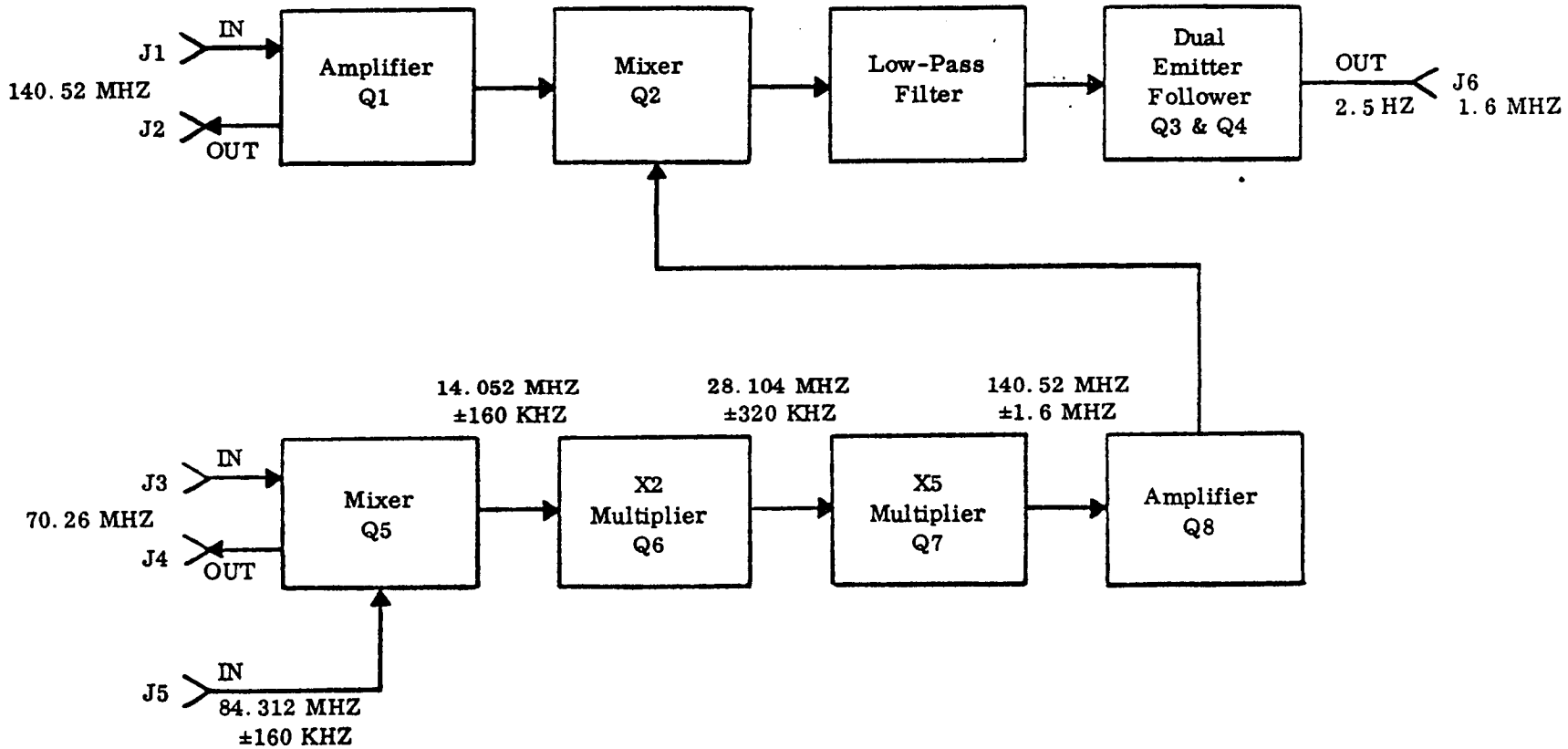


Figure 2-15. Block Diagram - Doppler Detector

TABLE 2-9

SPECIFICATIONS FOR DOPPLER DETECTOR

1.	Input Frequencies:	84.312 MHz Level 0 dbm 70.26 MHz Level +10 dbm 140.52 MHz Level +10 dbm
2.	Bandwidth -3 db:	2 MHz (all inputs)
3.	Tuning Range:	Fixed
4.	Input/Output Impedance:	50 ohms nominal
5.	Input/Output VSWR:	1.5:1 maximum
6.	Output:	2.5 Hz to 1.6 MHz (-3 db) Level +10 dbm
7.	Gain:	10 db ±2 db
8.	Input Signal Level Range:	See #1 above
9.	Output Level Signal Range:	+8 to +12 dbm
10.	Power Input:	+18 VDC @ 55 ma -18 VDC @ 35 ma DE9P Connector
11.	Size: Weight:	2 3/4" high x 3 7/8" wide x 9 1/2" long 2.5 lbs.
12.	Temperature:	25° C ±10° C minimum 0° C to 60° C design goal

back to the 2.342 MHz phase detector module, while the other output is the 2.342 MHz range tone which goes to the data extraction unit.

The phase-lock loop filter consists of a passive filter followed by an active filter. The passive filter consists of R7, R11, R14, R4 and C1 with relay K1 used to switch the filter bandwidth upon acquisition of a signal. The input of the passive filter comes directly from the phase detector module through Pin 8, J1. The output goes to the positive input of A1 in the active filter.

The active filter consists of A1, C2, R5 and R6. The output of this filter goes through a voltage divider R8 and R9 to the VCXO, A3. This VCXO is a Damon voltage controlled crystal oscillator centered at 2.342 MHz with an output level of 0 dbm, 50 ohms. It is variable over greater than ±500 Hz.

The transfer function of the VCXO is 500 Hz per volt.

The RF amplifier using Q1 provides a +10 dbm level at 50 ohms for the fine range tone at J2 for the Data Extraction Unit.

The second RF amplfier using Q2 provides a 0 dbm level of 2.342 MHz signal for reference in the 2.342 MHz Phase Detector Module.

The voltage which controls the VCXO is brought out through J1-14 to a front panel voltmeter to indicate the VCXO frequency above or below 2.342 MHz.

An emitter follower, Q3, is used to provide isolation for an analog voltage to MP1. This voltage varies from 0 to +5 volts and may be calibrated relative to frequency.

2.2.10 2.342 MHz Phase Detector Module

Figure 2-17 is a block diagram of the 2.342 MHz Phase Detector Module. Refer to Table 2-11 for specifications and to Figure 8-20 for a schematic of this module.

This module is designed to provide both a phase and a correlation detector output. It is very similar to the 4.684 MHz Phase Detector Module. The phase detector output is used in the #2 or 2.342 MHz phase-lock loop to synchronize the 2.342 MHz VCXO with the 2.342 MHz range tone.

The correlation output is provided by a similar detector in which the reference is phase shifted 90 degrees.

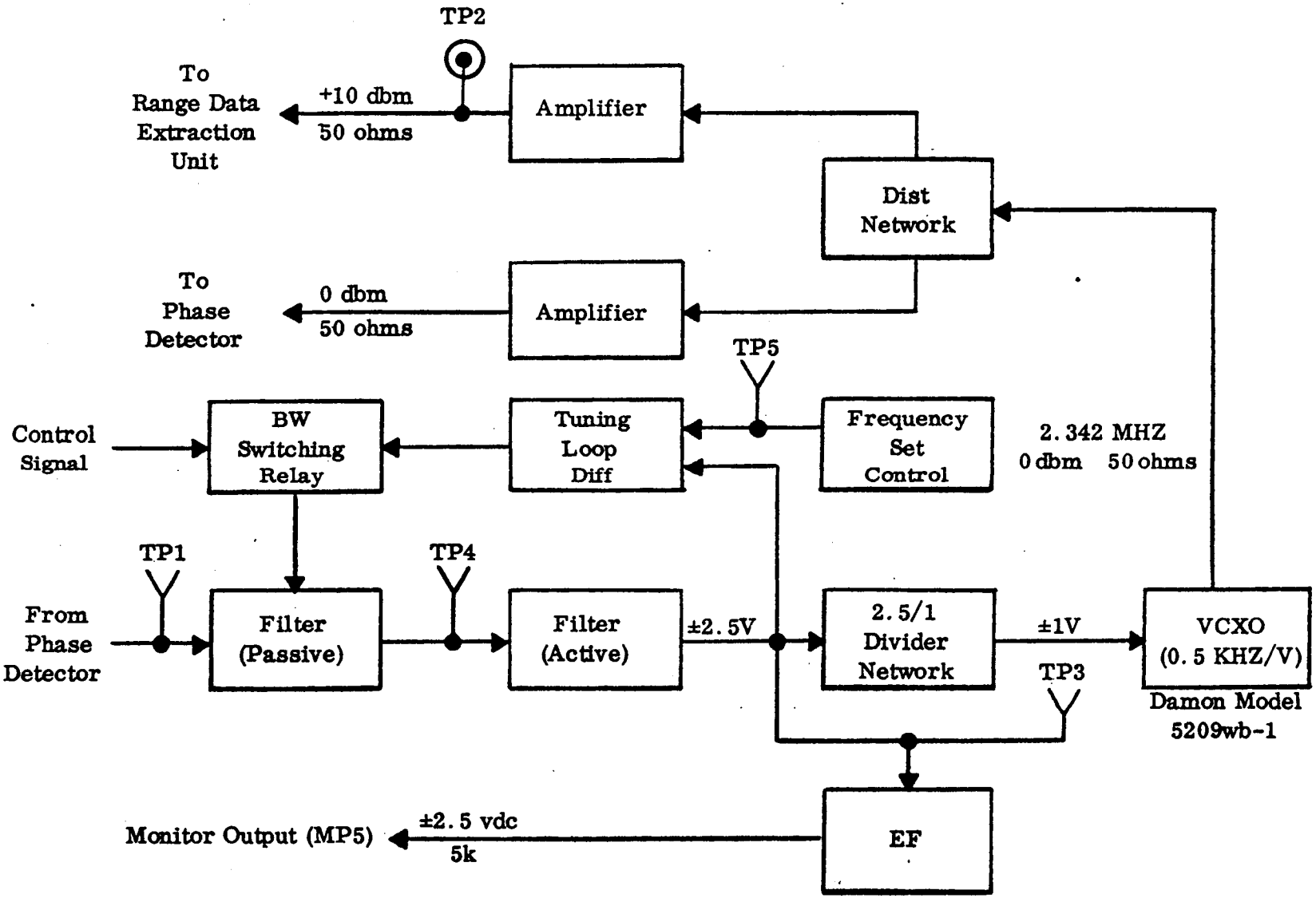


Figure 2-16. Block Diagram - VCO-2 Module

TABLE 2-10

SPECIFICATIONS FOR VOLTAGE CONTROLLED OSCILLATOR #2

1.	Inputs:	DC Control Signal .25 v/rad phase error		
2.	Outputs:	To Phase Det:	Frequency:	2.342 MHz
			Power:	0 dbm
			Impedance:	50 ohm
		External:	Frequency:	2.342 MHz
			Power:	+10 dbm
			Impedance:	50 ohm
		Monitor Point:	Voltage:	0 to +5 VDC
			Impedance:	5 K or less
3.	Closed Loop Bandwidth:	10 Hz (Loop Locked) 100 Hz (Loop Unlocked)		
4.	Power Input:	+18 VDC @ 22 ma -18 VDC @ 40 ma DA15P Connector		
5.	Size: Weight:	2 3/4" high x 3 7/8" wide x 9 1/2" long 3 lbs.		
6.	Temperature:	25° C ±10° C minimum 0° C to 60° C design goal		

Separate single stage amplifiers are provided on each input to each detector to provide the proper level and sufficient isolation between detectors.

The phase detector output is 0.25 volts per radian with about 7 millivolts input signals to J2.

The correlation detector output is handled by two separate amplifiers. A two-stage video amplifier which is essentially flat between 1 KHz and 75 KHz provides the range signals at J4 for processing in Range Signal Extraction Module. The DC component of the correlation output is filtered by a 20 Hz low pass filter and then amplified by a P65A Philbrick differential amplifier to provide about -4 volts DC to the acquisition circuit and to the associated correlation meter.

2.2.11 Range Signal Extraction Module

Figure 2-18 is a block diagram of the Range Signal Extraction Module. Refer to Table 2-12 for target specifications and to Figure 8-21 for a schematic of this module.

This module contains the range tone extraction circuitry for the 71.47 Hz, 2.2871 KHz and 73.1875 KHz signals. The video extraction channel is also contained on the module.

The input spectrum consists of a 73.1875 KHz signal, which is sometimes square wave modulated at a 1 KHz rate, and two lower frequency signals at approximately 1.1792 and 1.1078 KHz. The bandpass filter FL2 selects only the 73.1875 KHz signal and when modulated its first order modulation side frequencies. These are amplified in Q1. Bandpass filter FL1 is a narrower filter designed to pass only the 73.1875 KHz signal. Q2 provides additional amplification and Q3 provides necessary impedance matching to the load. A gain control (R10) is provided in the Q2 stage to set the output level.

When the 73.1875 KHz signal is modulated, it and its two first order side frequencies, are amplified in Q4 after passing through FL2. The video is then detected in CR1 and is amplified by Q5 and Q6, which also limits the signal to provide a cleaner output waveform. Emitter follower Q7 provides impedance matching to the load and also clamps the signal so that its furthest negative excursion is zero volts. R31 is the bias control which sets the clipping level. R34 controls the output signal level.

The two low frequency input signals are passed through a low pass filter consisting of C23, C24 and L7. The filter attenuates the 73.1875 KHz signals and prevents undesirable modulation of the 73.1875 KHz ranging tone by the two low frequency signals in the demodulator CR2.

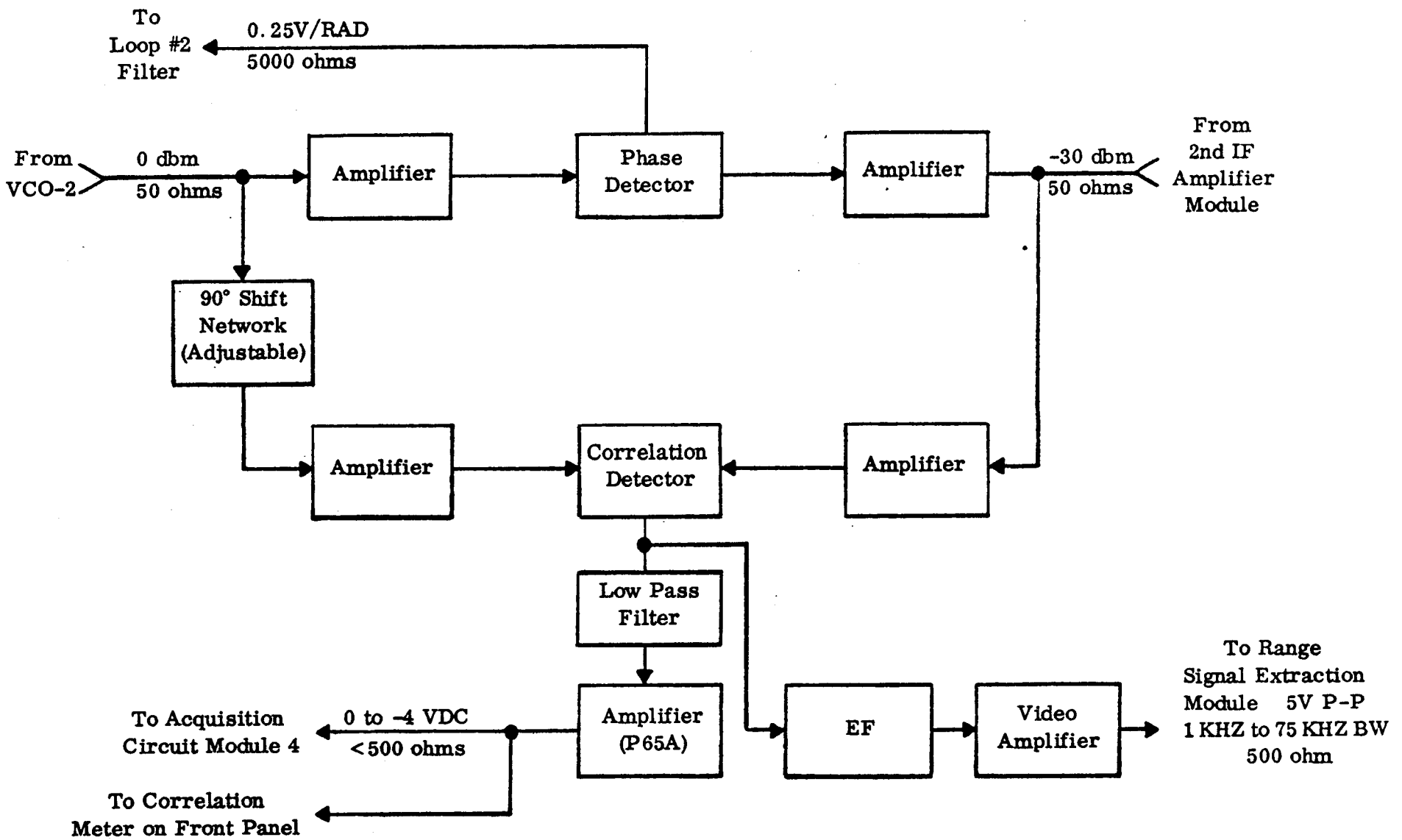


Figure 2-17. Block Diagram - 2.342 MHZ Phase Detector Module

TABLE 2-11

SPECIFICATIONS FOR 2.342 MHz PHASE DETECTOR

1.	Inputs:	Signal Input:	Frequency:	2.342 MHz
			Bandwidth:	±75 KHz
			Power:	-30 dbm
			Impedance:	50 ohms
		Reference Input:	Frequency:	2.342 MHz
			Power:	0 dbm
			Impedance:	50 ohms
2.	Outputs:	Correlation Detector:	Voltage:	-4.0 VDC
			Impedance	500 ohms
			BW	15 Hz
		Correlation Signal:	Voltage:	5 V p-p Nominal
			Impedance:	500 ohms
			BW:	75 KHz
		Phase Detector:	Sensitivity:	0.25 V/rad.
			Impedance:	5000 ohms
3.	Power Input:	+18 VDC @ 42 ma -18 VDC @ 42 ma DE9P Connector		
4.	Size: Weight:	2 3/4" high x 3 7/8" wide x 9 1/2" long 3.2 lbs.		
5.	Temperature:	25° C ±10° C minimum 0° C to 60° C design goal		

The latter signals are amplified in Q8 and beat together in demodulator CR2. The sum frequency at 2.2871 KHz and the difference frequency 71.47 Hz are extracted, filtered and amplified by their respective active filter channels. Q9 through Q13 comprise the higher frequency channel, and Q14 through Q18 comprise the lower channel. Both channels are identical except for frequency. In the 2.2871 KHz channel, Q9 is an emitter follower to prevent loading of the notch filter. Q10 is the amplifier stage of the first active filter. C31, C32, C33, R50, R51 and R52 form the Parallel-T feedback filter network which feeds back all frequencies except the desired center frequency. In this way, Q10 amplifies only what is not fed back. Two such feedback amplifiers have been cascaded to obtain steeper skirts and greater ultimate attenuations in each channel. Output amplifier followers Q13 and Q18 match the channel outputs to the 500 ohm loads. R66 in the 2.2871 KHz channel and R89 in the 71.47 Hz channel are used to adjust the output levels.

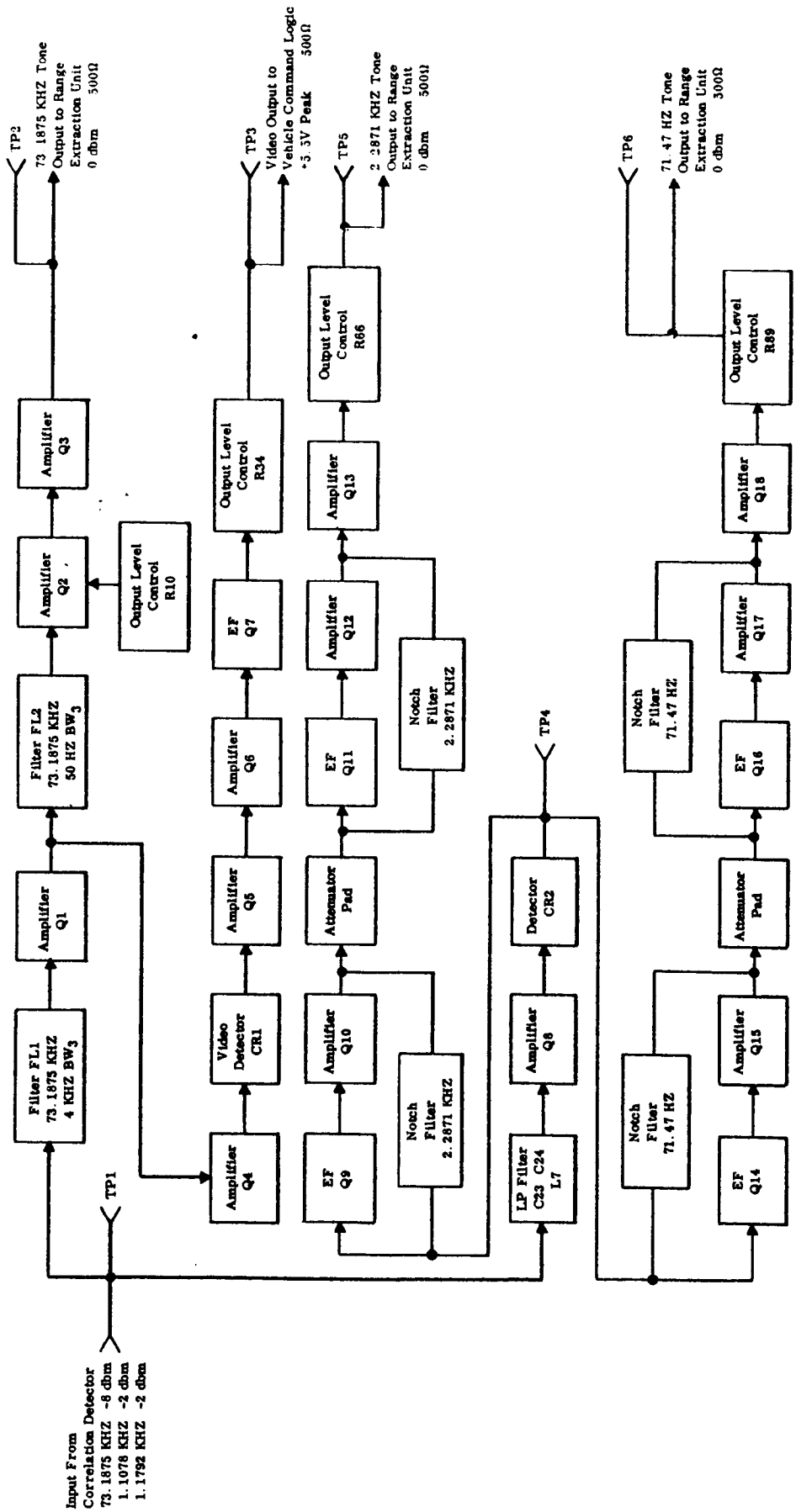


Figure 2-18. Block Diagram - Range Signal Extraction Module

TABLE 2-12

SPECIFICATIONS FOR RANGE SIGNAL EXTRACTION MODULE

1.	Input Spectrum:	DC 0 to -3 volts 1.10782 KHz -2 dbm (Approximately) 1.17929 KHz -2 dbm (Approximately) 73.1875 KHz -8 dbm (Approximately)
2.	Input Impedance:	500 ohms
3.	Input Connector:	Microdot 31-50
4.	Output Signals:	Video, 1 KHz, +5.5 ±0.1 V peak 73.1875 KHz, 0 dbm, 500 ohms 2.287+ KHz, 9 dbm, 500 ohms 71.47+ Hz, 0 dbm, 500 ohms
5.	Output Connectors:	Microdot 31-50
6.	Output Impedance:	500 ohms each output
7.	Output Bandwidth: (3 db)	Video Channel Approximately 2 KHz 73.1875 KHz Channel 100 Hz 2.287+ KHz Channel 100 Hz 71.47' Hz 50 Hz
8.	Test Points:	TP1 Input Signal TP2 73+ KHz Output TP3 1 KHz Video Output TP4 71 Hz and 2.28 KHz Tone Demodulator Output TP5 2.28+ KHz Output TP6 71+ Hz Output
9.	Power Input:	+18 VDC @ 100 ma -18 VDC @ 10 ma DE9P Connector
10.	Size: Weight:	4 1/4" high x 3 3/4" wide x 9 1/2" long 4 lbs.
11.	Temperature:	25° C ±10° C minimum 0° C to 60° C design goal

3.0 RESULTS OF TESTS

It is unfortunate from the ITTFL point of view that neither a frequency synthesizer nor signal simulator was GFE for use in testing the receiver, nor was funding provided for the building of these much needed pieces of test equipment, which are very special to this program, and would not normally be found in any well equipped electronics laboratory. As a result, ITTFL could not be responsible for the final results produced by the receiver, since it was impossible to properly test it.

Due to the rush to ship the first channel (Channel No. 2) as quickly as possible, and due to the lack of the proper auxilliary equipment, few tests were made beyond trying to ascertain that the phase-lock loops operated properly and that the range tone signals appeared at their outputs.

More complete tests were performed on the second channel to be shipped (Channel No. 1), but since the common first i-f module was shipped out with Channel No. 1, more limited tests were again made on Channel No. 3. Tests results for Channel No. 1 and No. 3 are reproduced in Appendix A.

During the testing of Channel No. 2, the first channel to be assembled, the lack of a frequency synthesizer proved particularly troublesome. This was caused by the fact that the 3rd i-f frequency of 4.684 MHz was just one-half of the 3rd mixer L.O. signal of 9.368 MHz. Due to this, the beat between the 9.368 and 4.684 MHz i-f signals in the 3rd mixer produced a signal which had a low frequency beat with the 4.684 MHz i-f signal. If the 9.368 MHz signal had been phase coherent with the 4.684 MHz reference signal, as it would be when using a frequency synthesizer, the beat note referred to above would have been zero, and thus would have given no trouble. However, considerable time was required to determine the cause of the beat note, which first was taken to be due to an oscillation in one of the amplifiers, and then to learn to live with it. Best results were obtained by deliberately detuning the generators so that the beat note had a frequency of several KHz.

One of the major troubles experienced in the testing of Channel No. 2 was limiting in the signal-to-noise ratio measuring channel. This limiting was not corrected in Channel No. 2, as it was decided to ship the unit "as is" and retrofit the correction at a later time. The required corrections were incorporated into Channels No. 1 and 3.

When testing of Channel No. 1 was started, it was decided that the input signal spectrum could be improvised by amplitude modulating one signal onto another. This provided double sidebands instead of single sidebands in most cases. But, it did allow introduction of required signals into the receiver, even if not at the proper relative amplitude levels.

An external diode modulator was used to modulate a 2.342 MHz signal on the main i-f carrier of 96.9588 MHz (for Channel No. 1). This provided a double sideband modulation, but the unwanted sideband was filtered out in the receiver i-f amplifier. As indicated on a spectrum analyzer, the carrier 2.342 MHz below the main carrier was about 3 to 6 db below the main carrier. (In the AROD system these should have equal amplitudes.)

The deficiency of the 2.342 MHz signal caused by the reduced amplitude was corrected by increasing the 2.342 MHz output as described in Section 2.1.5.

The 2.342 MHz signal was provided by a Hewlett Packard Model 606 signal generator which has provisions for amplitude modulation from an external signal. The 1.107 and 1.179 KHz modulation frequencies were supplied by two audio generators. The 73.1875 KHz frequency was supplied by another HP606 signal generator. This was amplitude modulated as required in the video output tests by a 1 Kc square wave. The HP606 generator is not rated for modulation at frequencies above 50 KHz. The 73.1875 KHz signal did provide modulation, but the sidebands were unsymmetrical, showing some angle modulation along with the amplitude modulation. Only the two 1 KHz sidebands or the 73.1875 KHz sideband was modulated onto the 2.342 MHz signal at any one time, so tests did not indicate any problems which might be obtained from the three sidebands being present simultaneously.

During the testing of Channel No. 1, some of the deficiencies of the receiver showed up. Some of these were corrected, which involved relatively minor circuit changes. However some areas did show up where more complicated changes would be required. These are listed in Section 4.0 as areas where improvements could be made.

Changes were made in the following areas of Channel No. 1. These changes were also incorporated into Channel No. 3.

a. The mixer which produces the 2.342 MHz signal in the 2nd i-f amplifier module also provides the source of signal from which the signal-to-noise ratio detector operates. The amplifier preceeding this detector was limiting on the strong noise present at low received signal levels. Rather than provide a transistor capable of supplying the high noise power level, one stage of amplification was removed from ahead of the detector. An additional stage of amplification was then added after the detector. This allowed the noise output from the detector to rise linearily to the level of signal representing the phase-lock loop threshold.

b. Limiting was also found in the noise amplifier stages located in the PLL Filter Module. One stage was eliminated and the output stage redesigned to handle a greater dynamic range of signal. This then provided a maximum output from the noise detector of over 5 volts, as required for the signal-to-noise ratio monitor point. A separate detector to drive the Schmitt trigger circuit which indicates when the signal-to-noise ratio is below a pre-set value was eliminated and this circuit was driven directly from the analog output of the noise detector. This provided a range of adjustment from less than 10 db signal-to-noise to over 40 db signal-to-noise in the point where the indicator would change indication. (Signal-to-noise ratio being that in the 100 Hz phase-lock loop bandwidth.)

c. The demodulated signal amplifier in the 2.342 MHz correlation detector was modified to provide a gain control and a greater dynamic range to reduce possible intermodulation among the three signal frequencies.

d. The output amplifiers of the range tone signals were modified to provide more gain so that a lower value of driving signal could be used, thus further reducing the possibility of intermodulation among the three frequencies derived in the 2.342 MHz correlation detector.

Testing of Channel No. 1 also showed up a large amount of noise in the pulse video output. Time did not permit a further investigation into this problem until Channel No. 3 was in test. It was then determined that the top and bottom of the pulses could be preserved in spite of the noise by providing clipping in the pulse amplifier. However, the noise, at low signal levels, caused the time at which the rise or fall of the pulse occurred to jitter. It is recommended that this change be retrofitted to both Channels No. 1 and 2.

4.0 RECOMMENDATIONS

Three changes in the receiver design are recommended for improving performance.

a. The 2.342 MHz signal produced by the diode detector should have automatic gain control (independent of the i-f amplifier AGC) applied. The level of this signal is not constant since the efficiency of the diode detector varies with input signal-to-noise ratios decreasing as the noise increases above the signal level. In applying AGC to this signal, care must be taken that the phase shift with change in AGC is a minimum. One degree would be about the maximum tolerable, and even that much would start to interfere with obtaining the desired measurement accuracy. It is recommended that a voltage controlled attenuator be used as the controlling element, rather than applying AGC voltage to transistors. ITTFL has built voltage controlled attenuators having an unmeasurable phase shift (less than 1 degree) over a 30 db attenuation range.

b. As discussed in Section 3.0, the bandwidth of the 2.287 KHz filter must be reduced in order to reduce the 71.74 Hz sidebands. This will require a phase-lock loop rather than the feedback filter. The phase-lock loop should require little or no more space than the feedback filter.

c. If bandpass filters continue to be used to separate out the 73.1875 KHz sidetone, the range signal should not be permitted to pass through two filters in series as is now being done. This puts the phase shifts of both filters into this signal. Since phase shift to the video signal is of little consequence, no effort is made to produce a low-phase shift filter for this circuit. But the range tone filter must have a low-phase shift across that portion of the passband actually occupied by the signal. Hence this should not be degraded by being put in series with the other filter.

The following changes are also recommended in order to make possible the reduction of volume in the flight hardware.

a. The 73.1875 KHz filters are much too bulky to permit microminiaturization. It is recommended, therefore, that they be replaced by a single phase-lock loop. A correlation detector associated with this phase-lock loop can provide the demodulated video output. In order to reduce the noise content of the video at low signal levels, a low pass RC network having a 1 Kc break frequency should be used on the output.

b. Since the capacitors required in the 71.47 Hz feed-back filter are quite large, it may be more economical of space to use a phase-lock filter for this range tone also. Since both the frequency excursion and rates in this loop, as well as in the 2.287 KHz loop, will be very low, it will be possible to use a second order loop without introducing more than a 1 degree phase error.

5.0 INSTALLATION

Each of the receiver chassis is provided with slides which should be fastened in proper position in the receiver cabinet. Then pull out each slide as far as it will go. Each chassis may then be placed into the cabinet by engaging the slide members. After pushing the receiver chassis into the slides about three inches, they will lock, which is then the extended position of the slides. The chassis may then be tilted to any angle by releasing the catches on both sides, just in back of the front panel.

To push the receiver chassis all the way into the cabinet, turn the chassis to the horizontal position, push in the release buttons on each slide and push the chassis on into the cabinet.

> NOTE: When connecting cables to the receiver chassis enough slack must be allowed for withdrawal of the chassis and turning it.

All coaxial cables connect to individual TNC coaxial connectors on the chassis rear apron. All DC and low frequency signal leads are brought out to the multiple pin connector on each chassis. Refer to schematics of Figures 8-1, 8-3, 8-4 and 8-5 for the proper cable connection points.

DC lines should be connected with No. 16 gauge wire. Low frequency signal lines may need shielded wire to prevent pick-up of interfering signals.

The RF amplifier and mixer components must be added to the power supply and 1st i-f amplifier chassis.

Both the +18 V and -18 V lines should be connected to each of the modules. It may be convenient to put a junction block in the cabinet (similar to those used in the channel chassis) to run the +18 V and -18 V leads to each chassis. The switch in the power supply chassis switches the DC output only. All power leads to the other chassis should be from the output of this switch (pins D and E on the multiple pin connector, J2 of the power supply chassis.

In running reference oscillator leads from the synthesizer, the following precautions should be noted:

a. The 4.684 MHz reference line must be divided four ways (one for each channel). Either resistive or reactive dividers may be used. If resistive dividers are used, no more than a total of 12 db reduction of power from the synthesizer output of +10 dbm shall be made for any one channel, providing

a minimum of -2 dbm signal to each channel. If a reactive divider is used, it may be necessary to add fixed attenuators to provide not more than +2 dbm of power to any one channel. Since only three channels have been provided, the fourth output from the dividers should be terminated in a 50 ohm resistive load. Figure 5-1 shows how three 6 db resistive dividers can be used for this division.

b. The 70.26 MHz line must go from the frequency synthesizer output directly to the first channel (may be any of the three channels). The 70.26 MHz output of that channel chassis must be connected to the 70.26 MHz input of the next channel, and so on. The 70.26 MHz output of the last channel used must be terminated in a 50 ohm load.

c. The 140.52 MHz line from the frequency synthesizer must be connected in the same manner as the 70.26 MHz line (see b. above).

d. All other outputs from the frequency synthesizer to the receiver go directly to the chassis input connector as they go only to one source. However, the 12.6468 MHz, 14.052 MHz and 19.4386 MHz outputs of the synthesidzer must be attenuated by means of a fixed (or adjustable) attenuator to provide the proper level of 2.342 MHz signal out of the 2nd i-f amplifier module, as described in Section 2.1.5. Approximately 10 to 20 db of attenuation will be required of each attenuator. The value used should be within 1 db of the value required to produce the proper 2.342 MHz output level (approximately 7 mv RMS) at J4 of the 2nd i-f amplifier module.

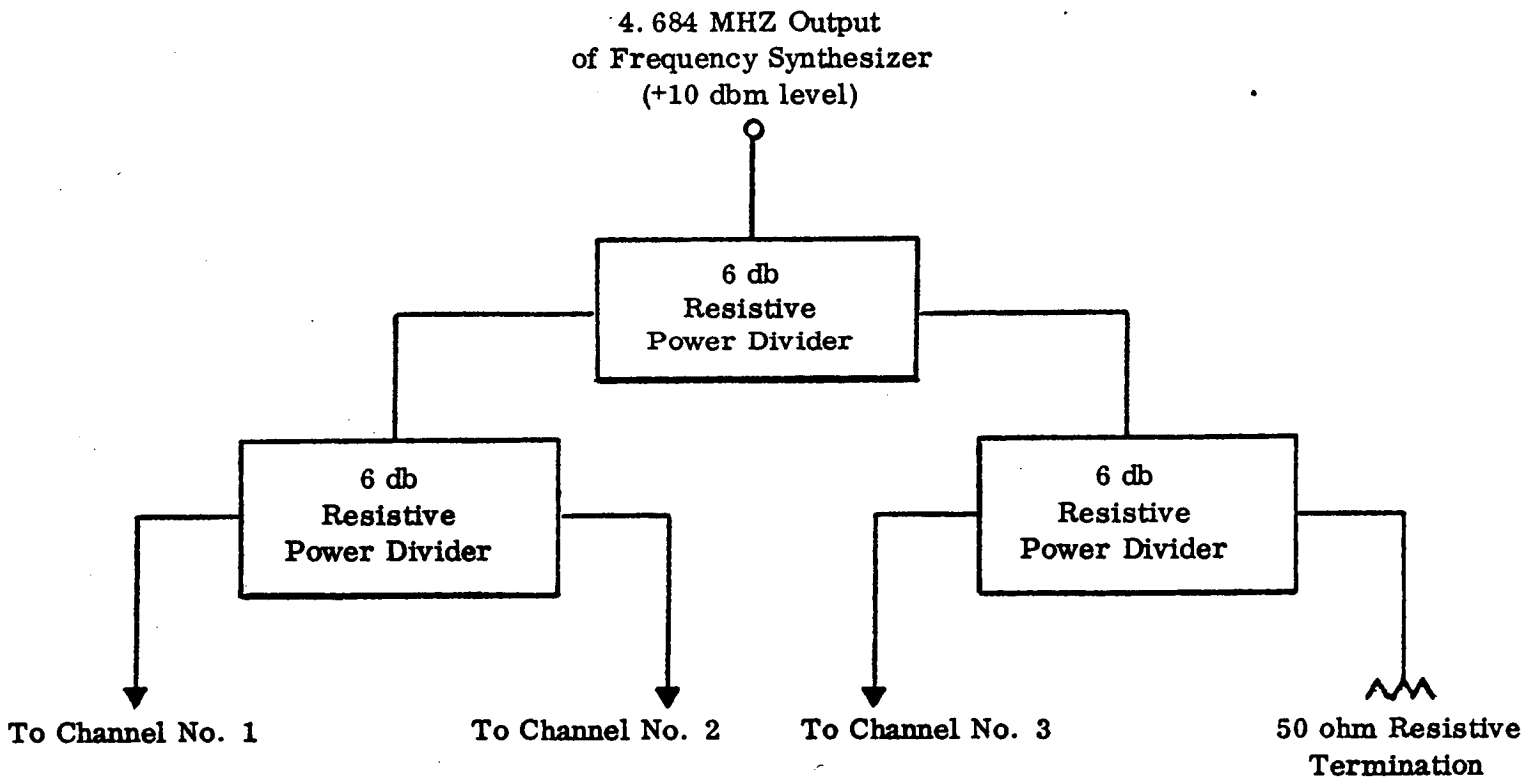


Figure 5-1. Power Division of 4.684 MHZ Output from Frequency Synthesizer

6.0 RECEIVER ALIGNMENT AND TEST

Provided that each module has been properly aligned as described in Section 7.0 of this manual, there are only a few adjustments that must be made on each channel chassis to insure proper operation of the receiver. While these adjustments were originally made at ITTFL before shipment of each chassis, it may sometimes be necessary to recheck them.

6.1 Test Equipment Required for Test of AROD Vehicle Tracking Receiver and Its Modules

Quan.	Manufacturer	Model	Description
2	Hewlett Packard	721A	DC Power Supplies
1	Boonton	91C	RF Voltmeter
1	Hewlett Packard	412A	DC VTVM
2	Kay	30/0 432C	Attenuators
1	Lavoie	LA-19	Spectrum Analyzer
1	Beckman/Berkeley	5350	Digital Volt Ohmeter
1	Hewlett Packard	608	RF Generator
2	Power Designs Inc.	5015A (or capable of ±18 V at 650 ma)	Transistorized Power Supplies
1	Special 2.342 Mc Signal Generator w/Phase Modulator		
1	Test Fixture w/Switch to Operate Relay K1		
1	Tektronics	531 w/Type B Plug in Unit	Oscilloscope
1	Hewlett Packard	524B w/Heads 526A, 525A and 525C	Frequency Counter
1	Technology Inst. Corp.	Type 320-A	Phase Meter
1	Hewlett Packard	606	Signal Generator

6.2 Manual Gain Control

To provide manual gain control, remove P2 from J2 of Module #2. Insert special test fixture shown in sketch of Manual Gain Control. See Figure 6-1.

6.3 Application of Power

Set positive and negative power supplies to 18 volts.

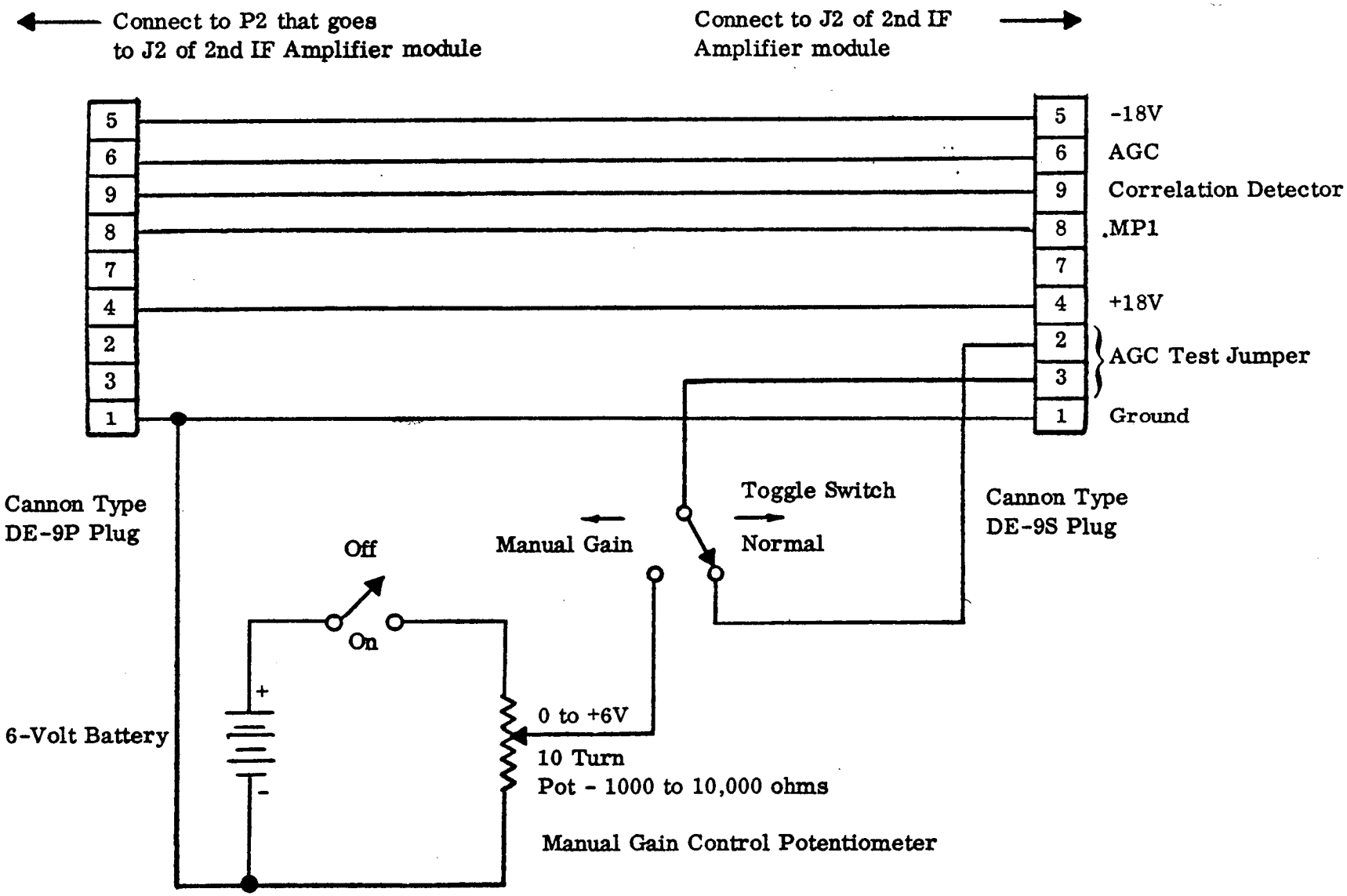


Figure 6-1. Manual Gain Control

Apply power and measure total current of each supply. Record

(+18 volt supply approximately 600 ma)
(-18 volt supply approximately 400 ma)

6.4 Meter Adjustments

6.4.1 4.684 MHz Loop Frequency Meter Calibration

Refer to Figure 6-2 for a schematic of this meter circuit.

With no power applied to receiver, adjust the mechanical zero setting of the frequency meter to obtain a zero reading (mid scale). Connect a HP 524-B Frequency Counter with Type 525-A Head to J3 of the VCO-1 module. Apply power.

a. Adjust R67 of the PLL filter module to obtain a frequency reading of 84.312 MHz on the HP counter. The front panel frequency meter should read zero.

b. If frequency meter does not read zero, readjust R67 of the PLL filter module to obtain a zero frequency meter reading and record reading obtained on the HP counter.

c. Adjust R67 of the PLL filter module to obtain reading on HP frequency counter 140 KHz higher than reading in Step b, or to 84.452 MHz if frequency meter read zero in Step a.

d. Adjust R13 on TB1 of receiver channel frame to obtain a reading on the front panel frequency meter 140 KHz higher than the reading in Step b.

e. Adjust R67 of the PLL filter module to obtain a HP frequency counter indication of 140 KHz below reading of Step b. Front panel frequency meter should read 140 KHz lower than the reading of Step b. If it does not, it is due to non-linearity of the VCO control characteristic and a compromise should be made to get the best average readings.

f. Readjust R67 of the PLL filter module to obtain a frequency counter reading of 84.312 MHz and leave it at this point.

6.4.2 4.684 MHz Loop, AGC/CORR Meter Calibration

Refer to Figure 6-3 for a schematic of this meter circuit.

To adjust CORR portion of this meter circuit, S2 must be in CORR position. Ground R10 on TB1 at C2 end. Adjust R7 on TB1 for maximum

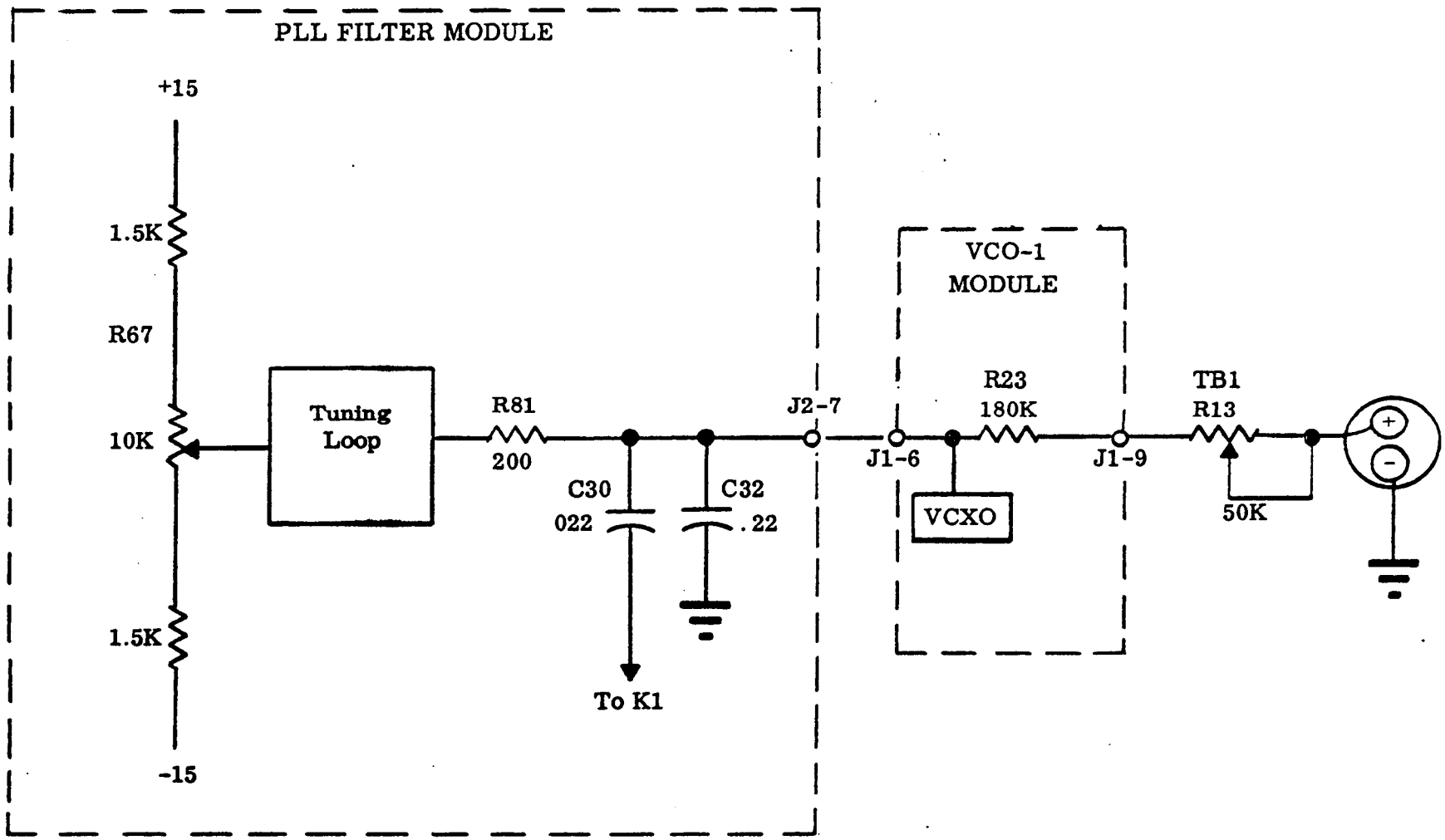


Figure 6-2. Meter Circuit 4.684 MHZ Loop VCO Frequency Meter

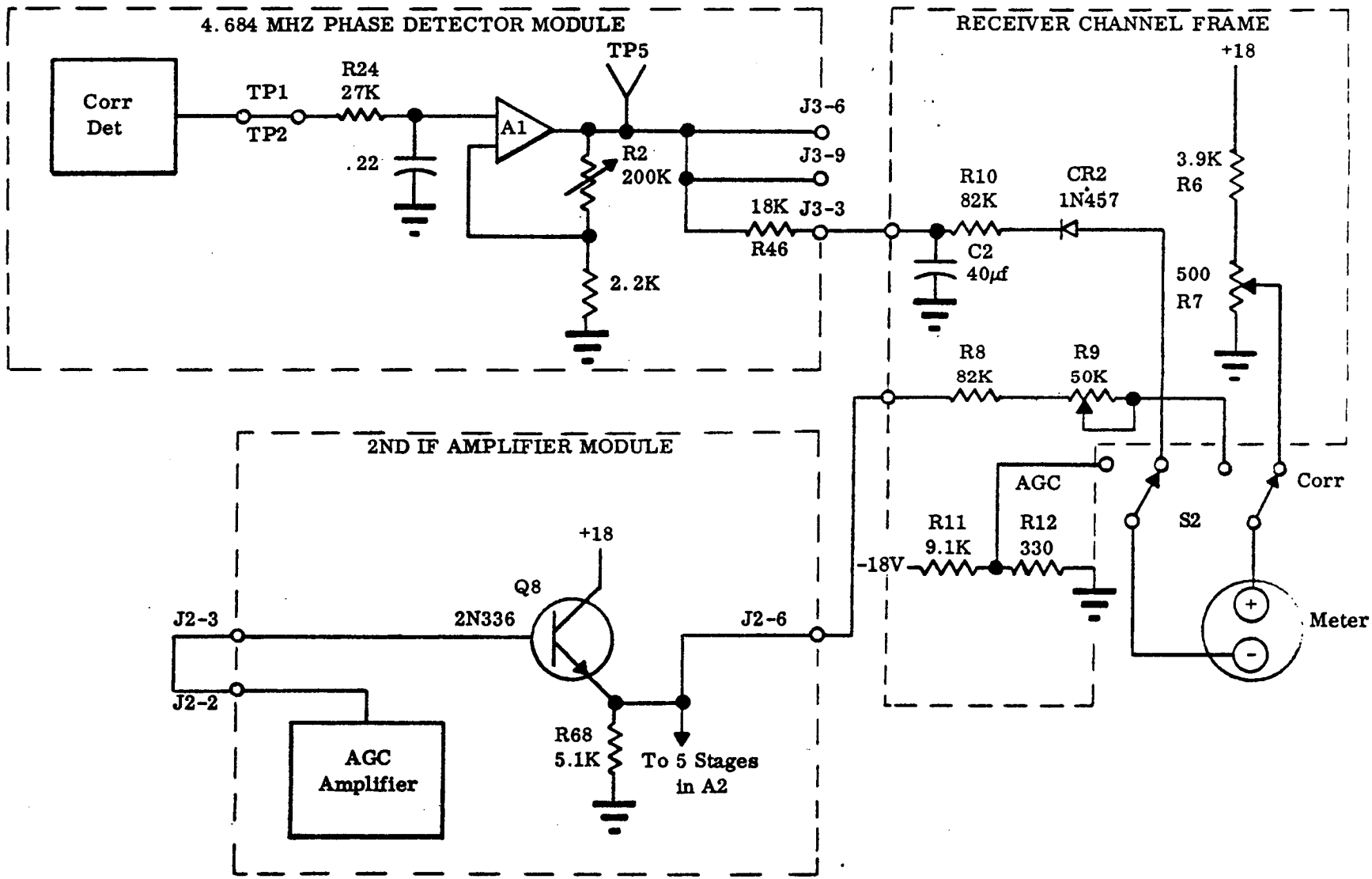


Figure 6-3. Meter Circuit 4.684 MHZ Loop - AGC/Correlation Meter

reading on meter then back off until meter just reaches a zero reading. Lock R7.

Remove ground from R10.

Loop at TP5 on 4.684 MHz phase detector module.

Remove jumper between TP-1 and TP-2 on 4.684 MHz phase detector module. Apply voltage from battery box to TP2 until TP4 is -4 volts. The panel meter should read 4 volts within 5%. If not tailor R10.

To adjust AGC circuit portion of AGC/CORR meter S2 must be in AGC position.

This meter is set to read the change in AGC buss voltage which ranges from slightly negative when the amplifier gain of the 2nd i-f amplifier module is maximum to about +5 volts when a strong signal is present and the phase-lock loop is acquired.

With no signal in, with AGC circuits operating, and with the RF modules operating in the receiver to provide the basic noise level, the AGC meter should read zero. If not tailor R12.

Next apply manual gain control and adjust to provide 4 volts between the input end of R8 and the junction of R11 to R12. Adjust R9 for a reading of 4 volts on the AGC meter.

6.4.3 Adjustment of 2.342 MHz Loop Frequency Meter

Refer to Figure 6-4 for a schematic of this meter circuit.

The adjustment of this frequency meter is similar to that of the 4.684 MHz loop. Mechanically zero meter (center scale) with power "OFF". Connect HP 524 Frequency Counter to J2 of the VCO-2 module. Apply power.

a. Adjust R3 of the VCO-2 module to obtain frequency reading of 2.34200 MHz on frequency counter. Front panel frequency meter should read zero.

b. If meter does not read zero, adjust R3 of the VCO-2 module to obtain a zero reading and record frequency indicated by counter.

c. Set R3 of the VCO-2 module to provide a frequency counter reading of 400 Hz higher than in Step b. Adjust R5 of TB1 on the receiver channel frame to obtain frequency meter reading of 400 Hz.

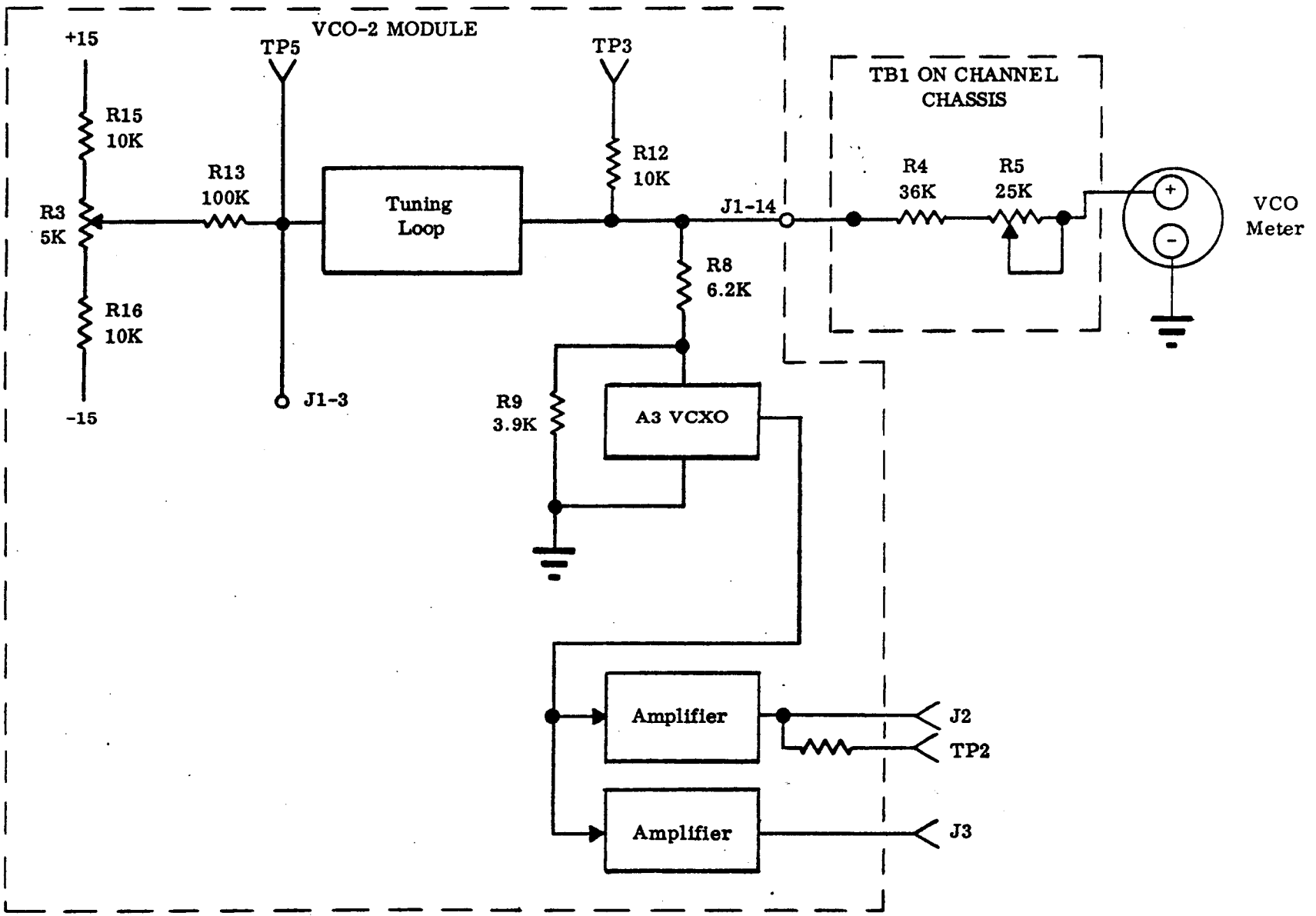


Figure 6-4. Circuit of 2.342 MHZ Loop Frequency Meter

d. Set VCO-2 module to provide a frequency counter reading of 400 Hz lower than obtained in Step b. Frequency meter should indicate -400 Hz. If it does not, a compromise will be necessary to get the best average readings.

e. Set R3 of VCO-2 module to provide a frequency counter reading of 2.342 MHz and leave it set at this point.

6.4.4 Adjustment of CORR Meter in 2.342 MHz Loop

Refer to Figure 6-5 for a schematic of this meter circuit.

First adjust mechanical zero on meter to zero with power "OFF."

With zero voltage at TP5 of the 2.342 MHz phase detector module (ground TP5) adjust R3 on TB1 until meter just reads zero. Remove ground from TP5.

Remove jumper from TP1 and TP2 on 2.342 MHz phase detector module and connect battery box voltage to TP2. Set this input (about -0.25 V) for -4 volts at TP5 of 2.342 MHz phase detector module. Meter on panel should read 4 volts within 5%. If not tailor R1. Replace TP1 and TP2 jumper.

6.5 Checkout of RF Signal Path

a. Switch to manual gain control.

b. Apply -50 dbm signal to 2nd mixer and filter module at J1 or at J3 on frame, or -90 dbm to 1st i-f amplifier module at J1. Refer to sketch of RF levels and frequencies, Figure 6-6.

c. Apply required reference signal to J11 on frame.

d. Apply 4.684 MHz reference signal to J12 on frame.

e. Apply +18 and -18 volt power.

f. Check RF amplitude at J2 and J3 of the VCO-1 module. Should be 0 dbm ±1 db with 50 ohm load.

g. Check frequency from J2 with frequency counter. Set to 84.312 MHz with R67 of PLL filter module.

h. Check signal level out of 3rd i-f converter module at J7. Manual gain control should control this level to any desired value between 7 mv and about 130 mv of 4.684 MHz signal.

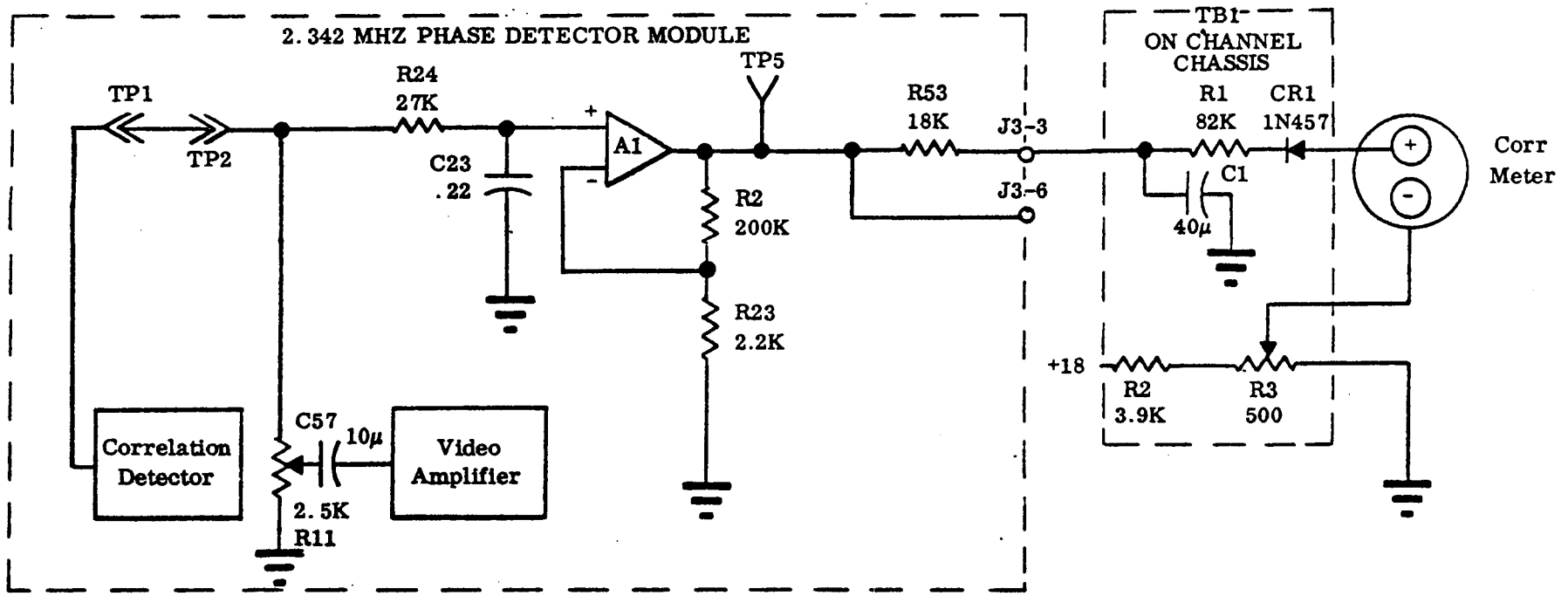
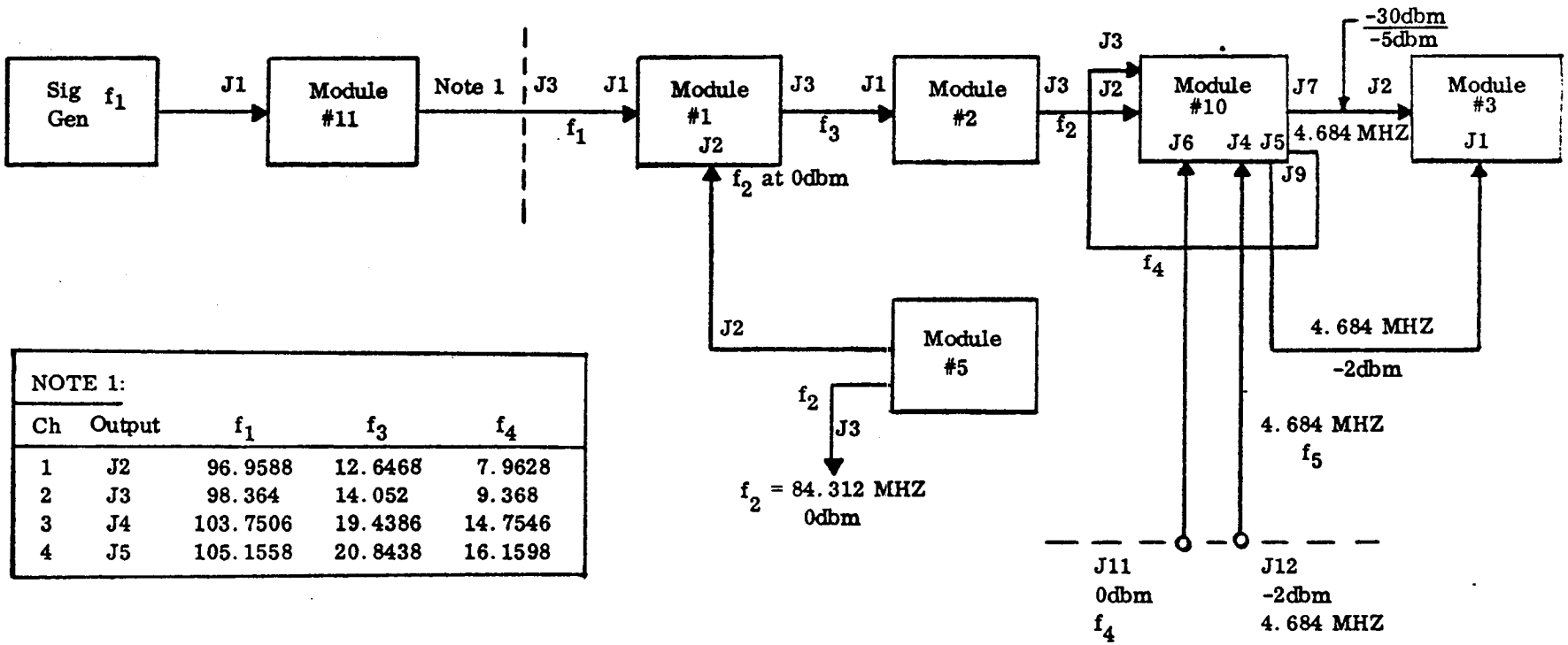


Figure 6-5. Circuit of 2.342 MHZ Loop Correlation Meter



NOTE 1:

Ch	Output	f_1	f_3	f_4
1	J2	96.9588	12.6468	7.9628
2	J3	98.364	14.052	9.368
3	J4	103.7506	19.4386	14.7546
4	J5	105.1558	20.8438	16.1598

Figure 6-6. RF Levels and Frequencies

i. Set manual gain control for 70 mv into J2 of the 4.684 MHz phase detector module. (At this point an oscilloscope connected to the correlation detector output at TP1 of the phase detector module will assist the operator in reducing the beat note to obtain lock-on. Also an amplifier and speaker connected to TP1 will assist greatly in tuning for zero beat and obtaining phase lock.)

j. Vary the frequency f_1 at the input to obtain zero beat and lock-on.

k. Refer to Figure 6-6 for RF levels and frequencies to trace for improper operation. (NOTE: Adjust all input signals to within less than 1 KHz.)

6.6 AGC Adjustments

Three adjusting pots are available on the 2nd i-f amplifier. R1, set for minimum change of phase with AGC voltage change. If this has not been set up, set R1 for maximum gain through the module with about 2 volts of AGC. R3 sets the DC level of AGC voltage and hence the i-f output level. R2 sets the i-f output level for uncorrelated AGC.

a. Apply the required input so that a -77 dbm level appears at J1 of the 2nd i-f amplifier module.

b. Insert "tee" connector at input J2 of 4.684 MHz phase detector module and connect RF voltmeter with high impedance probe.

c. Connect scope to TP3 of 4.684 MHz phase detector module. (Leave jumper in.)

d. Switch in manual gain.

e. Adjust input frequency for a low frequency beat note (about 100 Hz, but not close enough to lock-on).

f. Adjust manual gain control for one-half volt peak-to-peak on oscilloscope.

g. Read and record the r-f level at J2 of the 4.684 MHz phase detector module. This should be about 7 mv, and is the level at which the phase detector transfer function is 0.25 volts per radian phase error.

h. Without disturbing the gain control setting, adjust the input frequency to obtain lock-on.

i. Adjust R2 on the 4.684 MHz phase detector module to obtain a reading of 4 volts on the 4.684 MHz loop correlation meter.

j. Switch to AGC operation and adjust R3 on the 2nd i-f amplifier module to provide a reading of 4 volts on the 4.684 MHz loop correlation meter which should be the same as obtained in Step i.

k. Remove jumper from TP1 - TP2 of the 4.684 MHz phase detector module. (This opens the correlation AGC loop and allows the noise AGC to operate. It will also cause the acquisition light to go out, but should not cause a loss of acquisition with a strong signal.)

l. Adjust R2 of 2nd i-f amplifier module for 140 mv at J2 of 4.684 MHz phase detector module as read on RF voltmeter.

m. Replace jumper between TP1 and TP2 of 4.684 MHz phase detector module.

n. Check operation of receiver with weak input signals down to at least -140 dbm. The correlation output of the 4.684 MHz loop should not decrease below 3.5 volts at RF inputs (into 1st i-f amplifier module) of as low as -137 dbm. If the correlation output drops lower than 3.5 volts, R2 of the 2nd i-f amplifier module may need readjusting to allow more noise voltage to be present without cutting down the i-f gain through the noise AGC system.

6.7 Check AGC Time Constant

Apply 6 db square wave amplitude modulation at a low frequency rate about one-half Hz or less to the input signal. (Use amplitude modulator generator or external amplitude modulator.)

Observe AGC buss voltage on DC oscilloscope at Pin 6 of J2, on the 2nd i-f amplifier module. This voltage is available on R8 of TB1 back of front panel.

With a -100 dbm signal into the 1st i-f amplifier module or -50 dbm into the 2nd converter module, the AGC voltage should recover to 90% of its final value in about 300 milliseconds.

6.8 4.684 MHz Phase-Lock Loop

Reference frequencies must be provided to J11 and J12 on the back panel. The frequency to J12 is 4.684 MHz at a level of -2 dbm. The frequency to J11 depends upon the channel as follows:

Channel	Frequency
1	12.6468 MHz
2	14.052 MHz
3	19.4386 MHz
4	20.8438 MHz

6.8.1 Balance 4.684 MHz Loop Active Filter

While the phase-lock loop will operate to some extent if the amplifiers of the loop are not properly balanced, proper operation with low phase error can be obtained only with careful balancing of the DC amplifier zeros. The following procedure should be followed:

a. Check phase detector balance by removing input leads to J1 and J2 of the 4.684 MHz phase detector module. Open jumper between TP3 and TP4 on 4.684 MHz phase detector module and measure voltage at TP4 with a sensitive DC voltmeter (.1 volt or less, full scale). Voltage will be zero. Reconnect inputs to J1 and J2. With no signal applied to the receiver, the voltage at TP4 should still be zero (±1 mv). If not readjust C2 to obtain balance. Replace jumper between TP3 and TP4.

b. The DC amplifiers should have been balanced in the module alignment process, but change in power supply voltages might upset this slightly. To check this balance, apply a negative 4 volt signal to TP5 of the 4.684 MHz phase detector module. This will operate the relay which disconnects the tuning voltage. If any unbalance exists in the amplifiers, the front panel 4.684 MHz loop frequency meter will start traveling. (It may bounce around due to noise, but should stay at an average position.) Adjust R46 on the PLL filter module until the front panel 4.684 MHz loop frequency meter stays fixed at any point, but preferably near center scale.

6.8.2 Phase-Lock Loop Bandwidth

The phase-lock loop bandwidth may be checked, if desired, as follows:

a. Set input signal to amplitude sufficient to minimize phase noise at phase detector output.

b. Apply sine wave phase modulation of about ±20° to input signal.

c. Observe modulation sine wave from generator on one channel of a dual trace oscilloscope.

d. Observe phase detector output TP3 of 4.684 MHz phase detector module on the other channel of the same scope.

e. At frequencies well over 100 Hz the phase should be the same for both traces. Adjust the display for equal amplitude of each trace. A frequency stable generator must be used to keep noise on the signal to a minimum. Use external scope synchronizer from the low frequency generator.

f. To determine the 3 db video bandwidth reduce the modulation frequency till the phase error amplitude drops to .707. Another and perhaps more accurate method is to observe the point of 90° phase relation between the two traces. (The loop noise bandwidth is approximaely pi times the bandwidth observed above.)

6.8.3 Adjustment of Phase Control 4.684 MHz Loop

The correlation detector must be adjusted to 90° with respect to the phase detector.

a. With receiver operating lock onto a signal of medium amplitude.

b. Switch to manual gain control.

c. Set manual gain for about -0.25 volts DC at TP1 of 4.684 MHz phase detector module.

d. Adjust phase control pot, R1, on 4.684 MHz phase detector module for maximum negative voltage at TP1.

6.8.4 Pull In Range

a. With medium strength signal at input, move input signal to one side quickly to loose lock.

b. Count beat frequency at phase or correlation detector output TP1 or TP3 of the 4.684 MHz phase detector module.

c. Slowly reduce beat frequency while observing the count. At some frequency between 1 KHz and 2 KHz the phase-lock loop will suddenly pull in. Record the last frequency displayed on the counter.

d. Check pull in range on the other side by repeating the above procedure except the approach is made from the opposite direction.

6.8.5 Sensitivity

With loop locked reduce signal strength until acquisition starts to drop out.

Increase signal until the loop holds on for periods of at least five (5) minutes. This level may be defined as the threshold level.

The threshold level should be -140 dbm ±2 db.

6.9 2.342 MHz Phase-Lock Loop

The 2.342 MHz phase-lock loop may be checked with a 2.342 MHz signal from a signal generator as the signal source, although final check must be made with a signal simulator.

6.9.1 Balance 2.342 MHz Loop Active Filter

a. Remove jumper between TP1 and TP2 of 2.342 MHz phase detector module and apply a -4 volt bias to TP2. This will operate relay K1 in VCO-2 module.

b. Open TP3 and TP4 of 2.342 MHz phase detector module. Connect sensitive DC voltmeter to TP3 of VCO-2 module. Short TP4 of VCO-2 module to ground.

c. Adjust R1 on VCO-2 module to obtain zero volts at TP3 of VCO-2.

d. Remove ground from TP4 of VCO-2 module and adjust R39 on VCO-2 module to obtain a very low drift rate at TP3 near zero volts. This may also be observed on the 2.342 MHz loop front panel frequency meter.

e. Remove voltage from TP2 of the 2.342 MHz phase detector module and reinsert jumpers between TP1 and TP2 and TP3 and TP4.

f. Acquire signal and measure phase error voltage at TP3 of the 2.342 MHz phase detector module. This voltage should be at most.2 millivolts. If not, readjust R39 on VCO-2 module.

6.9.2 Measurement of Loop Characteristics

A scope or an amplifier and speaker may be connected to TP1 of the 2.342 MHz phase detector module to aid in monitoring loop operation.

a. Connect counter to J17 on back panel of receiver channel frame.

b. Connect signal generator to J2 of 2.342 MHz phase detector module.

c. Set input level to 7 mv.

d. Apply power.

e. Check and record pull in range in similar manner as in Section 6.8.4. (This range should exceed ±500 Hz.)

f. Next determine minimum input level at which loop will pull in when generator is first +400 Hz and then -400 Hz from center frequency. (The loop should lock-in within one second when a signal not exceeding 2 or 3 mv is suddenly applied at frequencies as much as ±400 Hz away from 2.342 MHz.) Record values.

g. Check bandwidth of filter (loop locked) as follows: (K1 of VCO-2 module not energized.)

h. Remove Q14 of PLL filter module to de-energize K1.

i. Use 7 mv, 2.342 MHz signal to J2 of 2.342 MHz phase detector module.

j. Phase modulate input signal to about ±20° with a frequency of 500 Hz.

k. Observe modulation at TP3 of 2.342 MHz phase detector module on one trace of a dual trace oscilloscope. The scope must be provided sync voltage from the audio generator. Apply modulating audio to the other scope trace. Adjust amplitude displayed on each trace to be equal. Phase difference should be zero.

l. Decrease frequency of phase modulation till phase difference is 90 degrees. Record this frequency. (The noise bandwidth of the phase-lock loop is approximately pi times this frequency.) This point should be about 30 Hz.

m. Replace Q14 of 2.342 MHz phase detector module.

n. Check narrow bandwidth in a similar manner. One exception is that the frequency of phase modulation at the start may need to be only 100 Hz. Record the frequency where the phase shift is 90 degrees. This should be about 3 Hz.

o. Check AM output response at J4 of 2.342 MHz phase detector module as follows.

p. Connect two 2.342 MHz signal generators to a 6 db "tee" pad and connect the output of the pad to J2 input on the 2.342 MHz phase detector module.

q. Set output signal levels to 14 mv on each generator.

r. Set one generator to 2.342 MHz and make sure the loop locks to this frequency.

s. Set frequency of second generator to 2.343 MHz and observe amplitude of 1 KHz difference frequency at J4 of 2.342 MHz phase detector module. Record amplitude.

t. Move frequency of second generator to 2.415 MHz. Record amplitude of 73 KHz at J4.

6.9.3 Adjusting 2.342 MHz Loop Signal Level

The signal input level to the 2.342 MHz loop should be adjusted as follows:

a. Lock the 4.684 MHz loop to a -100 dbm level received simulated transponder signal. Adjust the 2.342 MHz signal compnnent frequency so that the 2.342 MHz loop does not lock on. (A beat note of over 500 Hz will be required.)

b. Connect an oscilloscope to TP1 of the 2.342 MHz phase detector module. (Leave jumper between TP1 and TP2).

c. The amplitude of the beat note seen on the oscilloscope should be 0.5 volts p-p.

d. If level in Step c. is not proper, it can be changed by adjusting the level of the 12.6468, 14.052, or 19.4386 MHz reference signal applied to the receiver. An increase in the level of this reference signal will lower the level of the beat note.

NOTE: This adjustment will provide the proper level of 2.342 MHz signal at the given input signal level. As the input signal level is reduced, and especially at input signal levels approaching -130 dbm, the level of the 2.342 MHz signal will fall off. However, it should still give satisfactory performance to -130 dbm input signal levels.

7.0 MODULE ALIGNMENT AND TEST PROCEDURES

The following procedures should be followed in making alignment and tests of the individual AROD Vehicle Tracking Receiver Modules:

7.1 Alignment and Test Procedure for 1st i-f Amplifier

The first i-f Amplifier module is aligned in two parts or sections. The input section consists of one input amplifier with a pi coupler, a bandpass filter (5 section) and three cascaded video amplifiers with a pi output coupler. The output section consists of 5 outputs, a power divider and 5 output amplifiers with pi couplers.

7.1.1 Test Equipment Required

Quan.	Description	Manufacturer	Model #
1	Signal Generator	Hewlett Packard	608C
1	6 db Power Divider		
1	Slotted Line	Alford	2181-6
1	VSWR Meter	PRD	277B
1	Line Stretcher	Alford	B702B-N
1	Noise Figure Meter	Hewlett Packard	342A
1	Noise Diode	Hewlett Packard	343A
1	Power Supply	Hewlett Packard	721A
1	Counter	Hewlett Packard	524B
1	Counter Head	Hewlett Packard	525A
1	RF Voltmeter	Boonton Electronics	91C
1	Oscilloscope	Tektronix	567
1	Spectrum Analyzer	Lavoie	LA19
4	Special Cables - Microdot		
4	BNC Cables		
4	Microdot Adaptors	Microdot	BNC/Microdot

7.1.2 Input Section Alignment

Connect a signal generator to J1 input connector and an RF voltmeter to TP1. Set level high enough to give -47 dbm output. Set frequency to 100 Mc. See block diagram Figure 7-1 for Alignment and Test Set-up and schematic, Figure 8-2.

Adjust C2, C9, C10, C12, C13, C15, C16 and C92 for maximum output. Go over these adjustments at least 10 times to remove all inter-action. 45 db of gain should be realized with a smooth bandpass free of ripple and with no bumps on the slopes of the bandpass. This may be examined by careful inspection of the RF voltmeter while tuning the generator slowly through the bandpass. Connect the noise meter to J1 and TP1 and adjust C2 and L2 for best noise figure.

7.1.3 Completion of Alignment

Now connect TP1 and TP2 with a 50 ohm coaxial jumper. Connect the signal generator to J1 and tune to the desired frequency for each output shown on the block diagram of the module Figure 2-2. Set level to -81 dbm. Connect the RF voltmeter to each output alternately and tune the appropriate output pi section of each output for best gain. Each output should have the same gain ±1 db, but a separate bandpass for each channel.

After an operational module is obtained consult test schedule Table 7-1 for testing.

7.2 Alignment and Test Procedure for 2nd Mixer and Filter Module

The 2nd mixer and filter module is made up of 6 basic elements. Two input LC filters are aligned in module level tests. A balanced mixer is aligned in module test. The output amplifier requires no alignment. Two crystal filters are checked separately. Consult test and alignment block diagram for 2nd i-f mixer and filter module in Figure 7-2, and schematics Figures 8-6, 8-7 and 8-8.

7.2.1 Test Equipment Required

Quan.	Description	Manufacturer	Model #
3	Signal Generator	Hewlett Packard	608C
2	6 db Power Divider		
2	Line Stretcher	Alford	3702B-N
1	Diode Mixer		
1	Noise Meter	Hewlett Packard	342A
1	Noise Diode	Hewlett Packard	343A
1	RHO-TECTOR Bridge	Telonic	TRB-1
1	Power Supply	Hewlett Packard	721A
1	DC Voltmeter	Hewlett Packard	413A
1	RF Voltmeter	Boonton Electronics	91C
1	Spectrum Analyzer	Panoramic	SPA-3/25
1	Oscilloscope	Tektronix	567
1	Counter	Hewlett Packard	524B
1	Counter Head	Hewlett Packard	525A
1	Heat Cold Chamber	Tenney	
2	50 ohm loads		
4	Special Microdot Cables		
4	BNC Cables		
4	Microdot Adaptors	Microdot	BNC/Microdot

TABLE 7-1

1st i-f Amplifier Module Test Schedule

1.	Gain Test:		-20° C $+75^{\circ}$ C	Limit 50 db ±2 db
2.	Selectivity Test:	Center Frequency 99.886 MHz. Make Sel. Curve Record Points Down to -60 db. Output #5 only.	-20° C $+75^{\circ}$ C	Limit Nom. BW_3 ±28 ±14 MHz BW_{60} ±45 MHz
3.	VSWR Test: (Nom. Impedance 50 ohm Center BW_3)		-20° C $+75^{\circ}$ C	Limit Max. (1.5:1 BW_3)
4.	Noise Figure Test: (Output #5 Freq. 100 Mc)		-20° C $+75^{\circ}$ C	Limit 7 db Max. 5 db Desired
5.	Phase Test: (Linear Response BW_3)			Limit ±1% from Straight Line ±13 MHz
6.	Dynamic Range Test: (Each Output) Locate 1 db Compression Level			Limit min. 40 db -114/-84 dbm
7.	Intermodulation Rejection Test:			Limit 40 db ±5.5 MHz
8.	Power Supply Current Test:			Limit -18 V 25 ma
9.	Output Bandpass Test:	Channel 1 - 94.5/96.9 MHz Channel 2 - 96/98.4 MHz Channel 3 - 101.4/103.8 MHz Channel 4 - 102.8/105.2 MHz		Limit +4% -0%

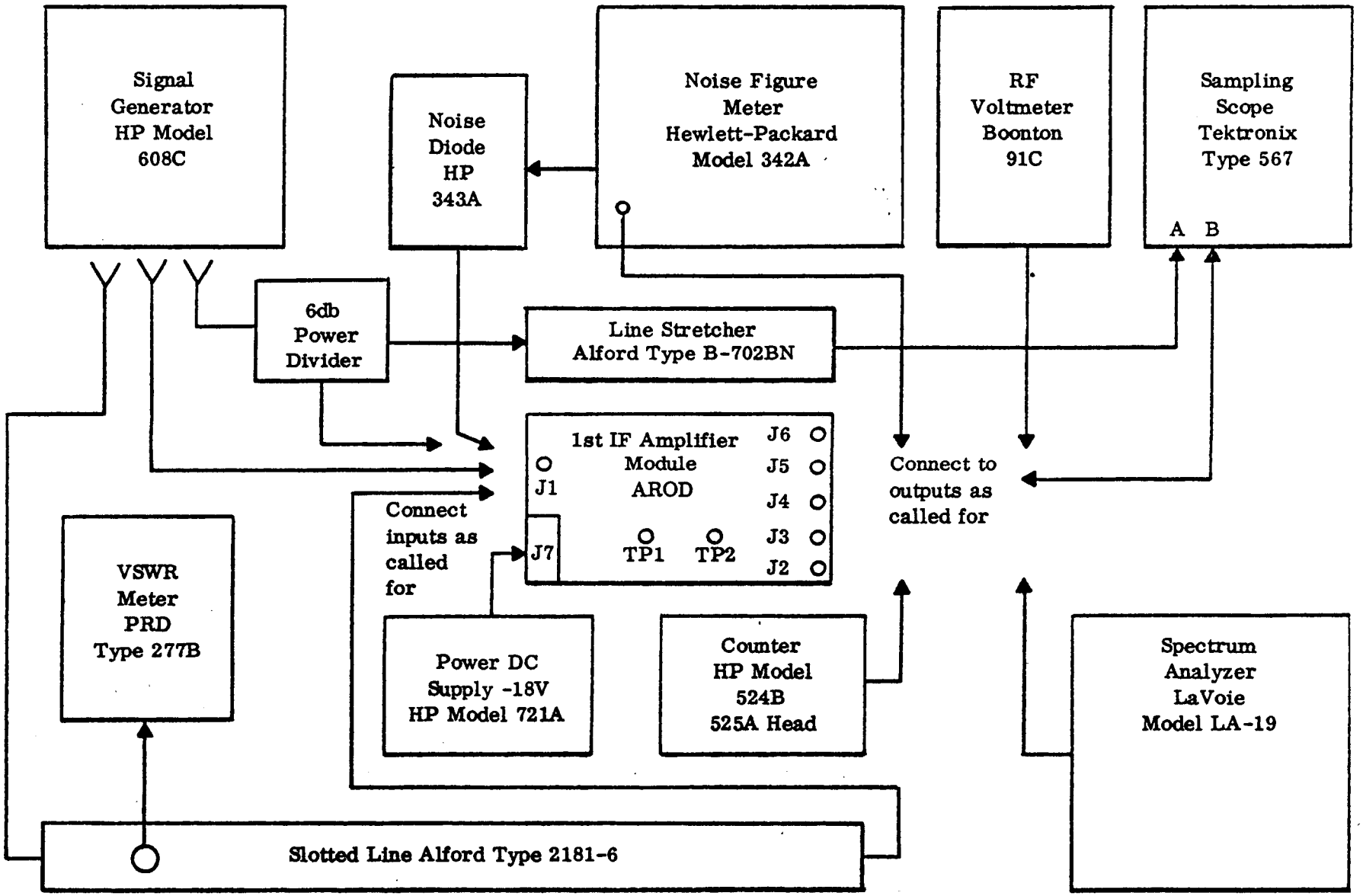


Figure 7-1. Alignment and Test Block Diagram for 1st IF Amplifier Module

7.2.2 Alignment

To align the signal input filter, connect a signal generator to J1 and set the frequency to the center frequency of the desired Channel 1, 2, or 3. Connect an RF Voltmeter to TP2 and terminate other connectors with 50 ohm dummy loads. Set signal generator output to full output and alternately adjust C1 through C10 several times for maximum output. When all inter-action is removed, check bandwidth which is greater than ±2.5 MHz.

To align the LO input filter connect generator to J2 and set frequency at 84.321 MHz and dummy load to J1. Alternately tune C11 through C20 removing all inter-action. Check bandwidth which is greater than ±1 MHz.

To align mixer stage connect two generators with a power divider to J1 and set at channel frequencies shown on schematic. Connect a third generator to J2 at 84.312 MHz and a level of 0 dbm. Connect an RF Voltmeter or sampling oscilloscope to J3. Set on low scale. Increase level of the first two generators until -42 dbm is read at the output. Tune frequencies for maximum outputs. Adjust C27, L12 and R4 and R6 for maximum output and cleanest waveform free of spurious effects. Adjust C27 and L12 with higher frequency generator at minimum output to optimize circuit for modulated carrier or wider bandpass filter. This is important for best phase response. Overall gain of module should be +2 db on wider carrier and 0 db on narrow carrier.

After an operational module is obtained, consult test schedule, Table 7-2, for testing.

7.3 Alignment and Test Procedure 2nd i-f Amplifier Module

The 2nd i-f amplifier has 3 basic sections for alignment. At module level test the filter is aligned in the module. Transformer T1 is aligned as well in module level test. Resistors R1, R2 and R3 can be pre-aligned at module level test but will finally be aligned in system test. Consult Alignment and Test block diagram for 2nd i-f amplifier module, Figure 7-3, and schematics Figures 8-9, 8-10 and 8-11.

7.3.1 Test Equipment List

Quan.	Description	Manufacturer	Model No.
2	Signal Generator	Hewlett Packard	606A
2	Power Divider 6 db		
1	Noise Meter	Hewlett Packard	342A
1	Noise Diode	Hewlett Packard	343A

TABLE 7-2

2nd Mixer and Filter Module Test Schedule

1.	Gain Test: (Both Outputs	-20° C +75° C	Unity ±2 db
2.	Selectivity Test: RF and IF Curves on Each Filter	25° C	±10 KHz ±100 KHz
3.	VSWR Tests: (Nom. Impedance 50 ohms center BW_3).	-20° C +75° C	< 1.5:1
4.	Noise Figure Test:	-20° C +75° C	Limit 10 db with 2nd i-f amplifier module following
5.	Phase Test: (Linear Response BW_3)		Limit ±1% from straight line
6.	Dynamic Range Test: (Output and TP3) Locate 1 db Compression Point		No compression -77/-31 dbm
7.	Spurious Output Test: Record any outputs greater than -60 db outside BW_3		< 60 db
8.	Power Supply Current Test:		Limit -18 V 10 ma

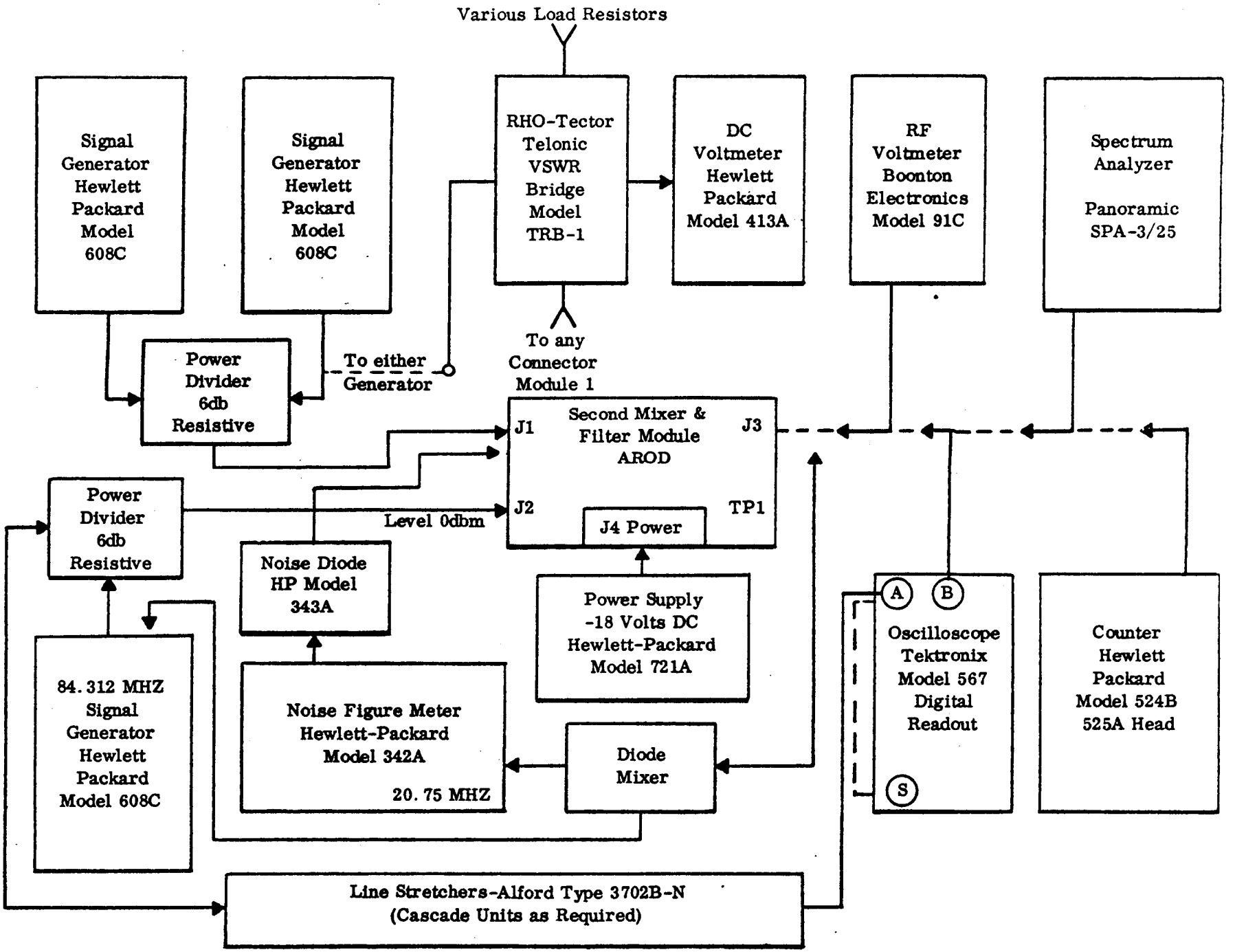


Figure 7-2. Alignment and Test Block Diagram - 2nd Mixer and Filter Module

7.3.1 Test Equipment List (Cont.)

Quan.	Description	Manufacturer	Model No.
2	Line Stretcher	Alford	3702B-N
2	Power Supply	Hewlett Packard	721A
1	Bias Supply 0-6 Volt		
1	RHO-TECTOR Bridge	Telonic	TRB-1
1	DC Voltmeter	Hewlett Packard	413A
1	RF Voltmeter	Boonton Electronics	91C
1	Spectrum Analyzer	Panoramic	SPA-3/25
1	Filter f_o 2.342 MHz		
1	Oscilloscope	Tektronix	567
1	Counter	Hewlett Packard	524B
1	Counter Head	Hewlett Packard	525A
2	50 ohm Loads		
4	Special Cables	Microdot	
4	BNC Cables		
4	Microdot Adaptors	Microdot	BNC/Microdot

7.3.2 Alignment

Connect two Hewlett Packard Model 606A, Signal Generators, to a 6 db power divider to combine their outputs. Connect the 3rd output of the power divider to J1 input to the module.

Adjust the level of both generators to -31 dbm. Assume alignment of Channel 2 for this discussion. Set one generator to 11.71 MHz frequency and the second generator to 14.052 MHz.

Connect the RF Voltmeter to J3 output connector and set range to give an indication.

Alternately adjust all capacitors in the filter for maximum output. Go back over each adjustment 10 times to remove all inter-action between capacitors. When the filter is properly aligned, no appreciable bandpass ripple will be present and both slopes will be symetrical with no humps.

Connect the manual bias box to Pin 6 of power connector J2. Apply 0 to +6 volts noting a decrease in output over the increased voltage range. Plot a curve of input level with constant output of -30 dbm against bias voltage.

Adjust R1 for maximum output at +2 V bias. This control will be finally adjusted in system test to give the most constant phase with change in AGC.

Connect a 2.342 MHz bandpass filter to J4 output and 50 ohm loads to J3, J5 and J6 outputs. Connect the output of the filter to an RF Voltmeter.

With both signal generators set to -77 dbm and on their respective frequencies and also bias to zero, adjust R2 for maximum output. The output should be near -30 dbm.

Connect a VTVM to Pin 2 of power connector J2 and ground. By changing generator levels a change in voltage should occur at Pin 2 of J2. If not, adjust R3 until this occurs. The DC voltage should vary 4 to 5 volts with changes in input generator levels from -77 dbm to -31 dbm.

After an operational module is obtained consult test schedule Table 7-3 for testing.

7.4 Alignment and Test Procedure for 3rd i-f Converter Module

The 3rd i-f converter is constructed with two separate printed boards. Each board is aligned separately and after completion both boards are checked as a unit test. Section one consists of a LC filter of a different center frequency for each channel into a balanced mixer stage, which requires alignment and then into a 4.684 MHz LC filter, a power divider and two output amplifiers which require alignment.

Block diagram, Figure 7-4, shows test set-up.

7.4.1 Test Equipment List

Quan.	Description	Manufacturer	Model #
2	Signal Generators	Hewlett Packard	606A
1	6 db Power Divider		
1	Switch Attenuator	Kay Electric 30-0	432C
1	RHO-TECTOR Bridge	Telonic	TRB-1
1	DC Voltmeter	Hewlett Packard	413A
1	RF Voltmeter	Boonton Electronics	91C
1	Spectrum Analyzer	Panoramic	SPA-3/25
2	Power Supply	Hewlett Packard	721A
1	Oscilloscope	Hewlett Packard	175A
1	Counter	Hewlett Packard	524B
1	Counter Head	Hewlett Packard	525A
4	Special Cables	Microdot	
4	BNC Cables		
4	Microdot Adaptors	Microdot	BNC/Microdot

TABLE 7-3

2nd i-f Amplifier Module Test Schedule

	Channel	Frequencies 200 KC	Frequencies 20 Kc	
1. Gain Test: Freq. Comb.	1	10.3048 MHz	12.6468 MHz	Limit 60 db ±2 db All outputs
	2	11.7100 MHz	14.0520 MHz	
	3	17.0966 MHz	19.4386 MHz	
	4	18.5018 MHz	20.8438 MHz	
2. VSWR Test: Record at all frequencies in No. 1 (above) Input and Output				Limit 1.5:1
3. Noise Figure: Use full gain				Limit 10 db
4. Phase Test: Linearity vs Frequency Linearity vs dynamic range at frequency in No. 1 (above)				Limit ±1% of a straight line plot
5. Dynamic Range Test: Composite of two signals any channel (See No. 1 above)				Limit 40 db -74/-34 dbm
6. Spurious Output Test: Record any output greater than -60 db outside BW				Limit -60 db
7. Selectivity Test: Determine frequencies where gain is down 3 db				BW_3 = 4.5 MHz
8. Voltage Tests: Record all voltages on all base, emitter and collector connections of all transistors with the following AGC voltages: Zero, +1 V, +2 V, +3 V and +4 V.				Record data in one table
9. Power Supply Current Test:				Limit +18 V 35 ma -18 V 35 ma
10. AGC Control Test: 10.3048 MHz 20.8438 MHz				

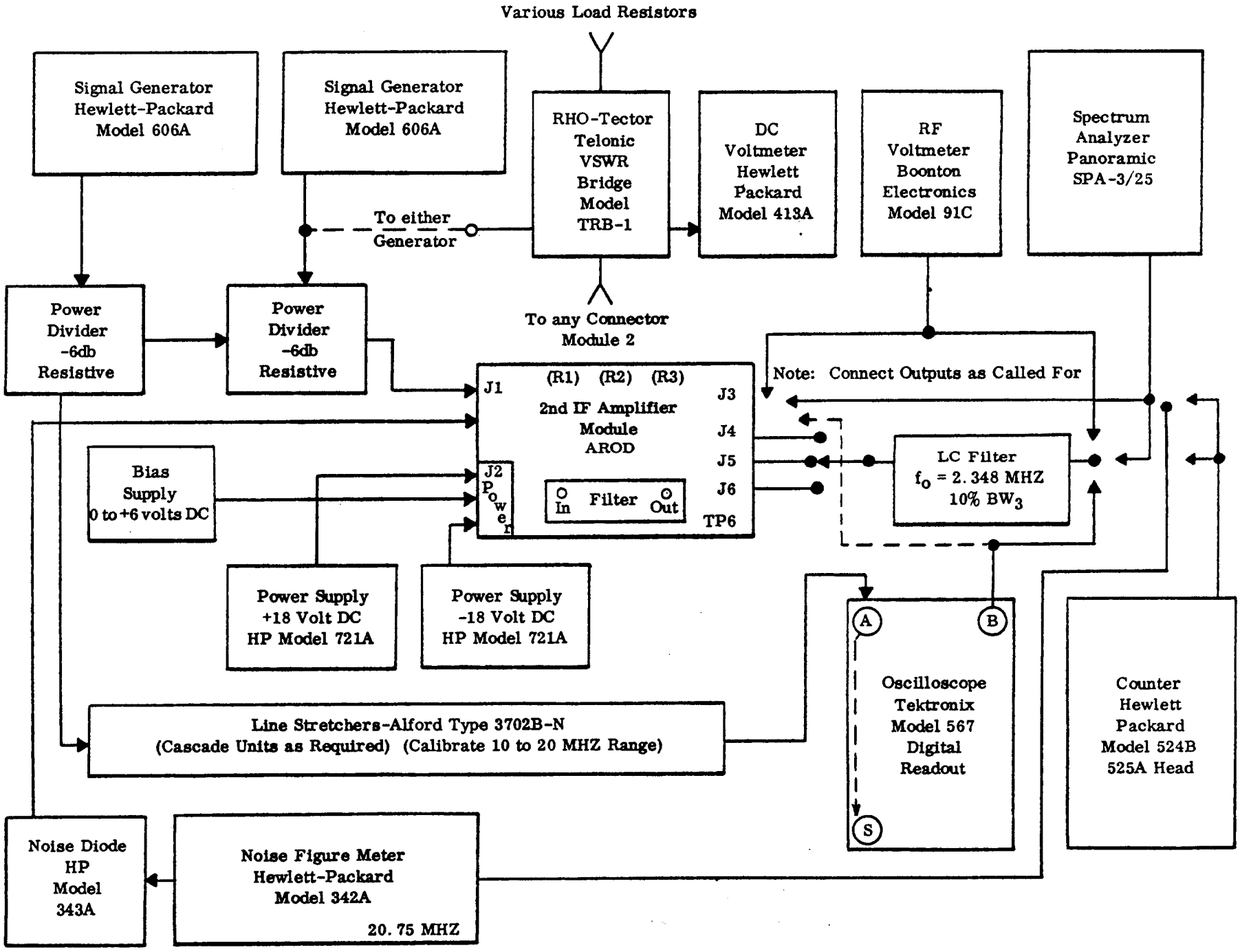


Figure 7-3. Alignment and Test Block Diagram for 2nd IF Amplifier Module

7.4.2 First Section Alignment

Connect two signal generators to J2 and J3 set on frequencies as shown on schematics Figures 18-12, 18-13 or 18-14. Each channel requires different frequencies. Set LO generator to -7 dbm and signal to -30 dbm. Connect oscilloscope to one output J7 connector and RF Voltmeter to second output J8. Adjust R7 for greatest output level. Sweeping the signal generator through the filter bandpass adjust C7, L3 for best bandpass symmetry and adjust C33 and C35 for greatest output.

7.4.3 Second Section Alignment

Connect a 50 ohm load to J5. Connect a 4.684 MHz generator to J4 at a -2 dbm level. Connect a second signal generator to J6 set at the channel frequency shown on schematics Figures 8-12, 8-13 or 8-14, set the level at 0 dbm. Check frequencies of generators with a counter. Adjust R18, L12, L13 and L16 for maximum output.

7.4.4 Final Check

Connect a coaxial line between J9 and J3. Connect generators to J6, J5 and J2 with proper channel frequencies and proper levels shown on the schematics. Connect RF voltmeter to J7 and J8 and verify operation.

After an operational module is obtained consult test schedule Table 7-4 for testing.

7.5 Alignment and Test for 4.684 MHz Phase Detector Module

Refer to Figure 8-15 for schematic of this module.

7.5.1 Test Equipment List

Quan.	Description	Manufacturer	Model #
2	DC Power Supplies	Hewlett Packard	721A
1	RF Voltmeter	Boonton Electronics	91C
1	DC VTVM	Hewlett Packard	412A
1	Oscilloscope	Tektronix	531
1	Signal Generator	Hewlett Packard	608
2	Attenuators	Kay 30/0	432C

7.5.2 Procedure

a. Remove jumper from TP1 to TP2. Remove jumper from TP3 to TP4. Set R1, C1 and C2 to approximate mechanical center.

TABLE 7-4

3rd i-f Converter Module Test Schedule

	Channel	Input Frequencies	
1. Gain Test:	1	12.6468 MHz	Input to output
	2	14.0520 MHz	0 db gain
	3	19.4386 MHz	
	4	20.8438 MHz	
	Output Frequency: 4.6840 MHz -30 dbm Input		
2. VSWR Test:	Record at frequencies given in #1 (above) Inputs & Output		Limit 1.5:1 to 50 ohms
3. Spurious Output Test:	Record any output -60 db outside -60 db BW		Limit <-60 db
4. Dynamic Range Test:			Limit >-5 dbm
5. Selectivity Test:	Determine -3 db, -6 db and -60 db. Record. Shape factor 6		Limit -3 db 1.16 MHz -6 db 1.52 MHz -60 db 9 MHz $SF = \frac{f_{BW60}}{f_{BW6}} = 6$
6. Voltage Test:	For reference only - Record: 1. All emitter DC voltages 2. All transformer RF voltages W/HiZ probe		
7. Power Supply Current:			Limit +18 V 10 ma -18 V 10 ma

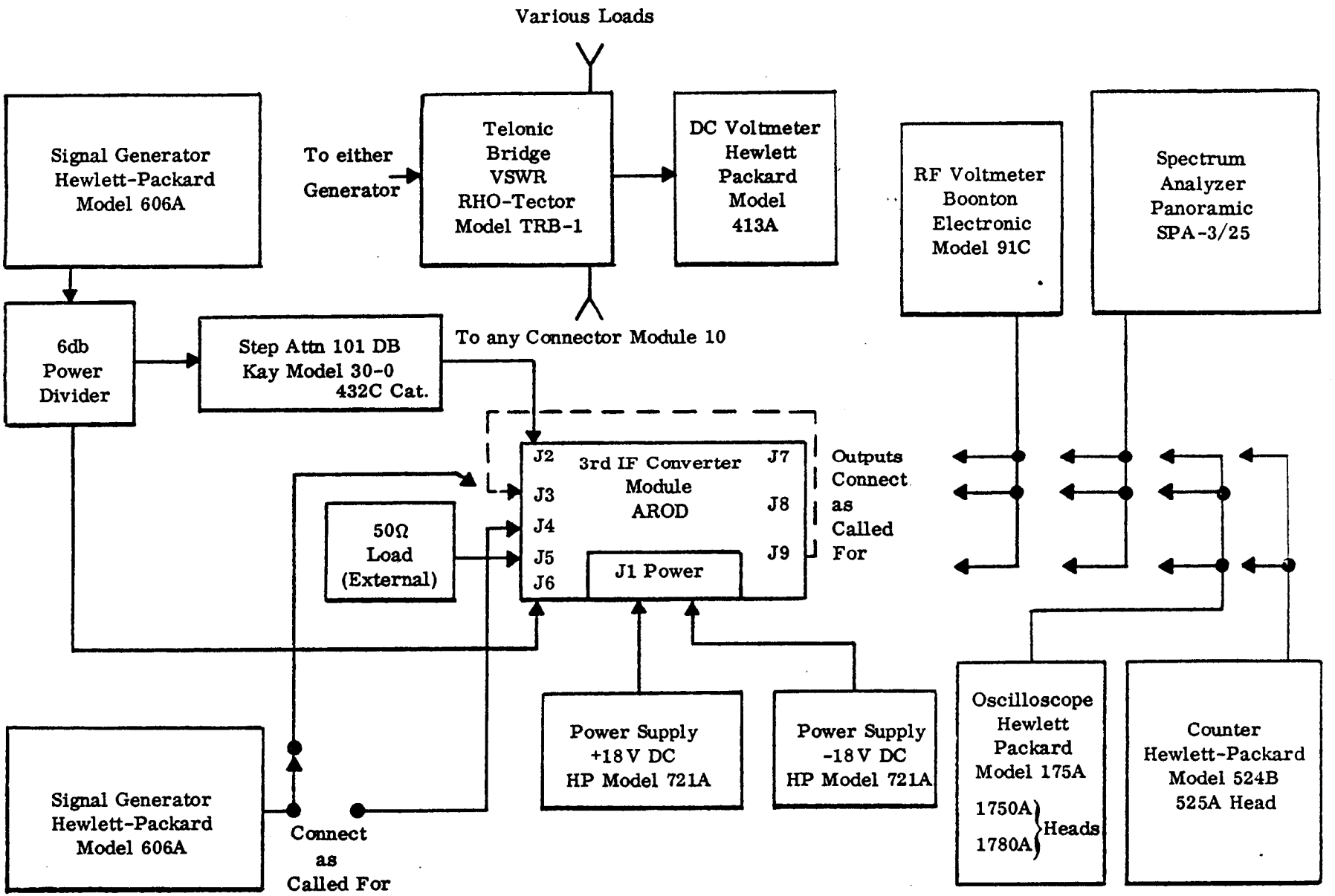


Figure 7-4. Alignment and Test Block Diagram for 3rd IF Converter Module

b. Apply +18 VDC and -18 VDC to J3.

c. Connect 4.684 MHz reference source (with attenuator) to J1.

d. Connect RF Voltmeter to J1 (use high impedance probe). Adjust reference input level to 223 mv RMS.

e. Connect 4.684 MHz signal generator (with attentuator) to J2. Connect RF Voltmeter and adjust signal input level to 7 mv RMS.

f. Connect oscilloscope to TP1 and adjust signal generator frequency control to approximately 100 cps either side of 4.684 MHz. (Observe 100 Hz beat note on scope.)

g. Tune T4 and T3 for maximum beat note amplitude.

h. Decrease reference signal input until beat note amplitude is approximately 1/10 the value observed after completion of Step g.

i. Tune T1 and T2 for maximum beat note amplitude (It may be necessary to repeat Step h. several times while tuning T1 and T2 for maximum.).

j. Repeat Step d.

k. Connect oscilloscope to TP4 and adjust T5 for maximum beat note amplitude.

l. Decrease reference signal input until beat note amplitude is approximately 1/10 the value observed after completion of Step k.

m. Tune T6 for maximum beat note amplitude. (It may be necessary to repeat Step l. several times while tuning T6.)

n. Repeat Steps c, d and e.

o. Connect Oscilloscope to TP4. Adjust 4.684 MHz signal input level (7 mv RMS ±0.5 mv RMS) until the beat note amplitude at TP4 is equal to 0.5 volt p-p. (0.25 V/Rad) (Tailor R14 if necessary.)

p. Connect d-c voltmeter to TP4. Adjust C2 for d-c balance (±1 mv d-c). (Tailor R44 if necessary to obtain the required balance.) (R44 may be placed in series with R6, R7, R8 or R9 as required.)

q. Connect d-c voltmeter to TP1. Adjust C1 for d-c balance (±1 mv d-c). (Tailor R45 if necessary to obtain the required balance.) (R45 may be placed in series with R30, R31, R32 or R33 as required.)

r. Disconnect signals from J1 and J2.

s. Connect jumper from TP1 to TP2.

t. Connect d-c voltmeter to TP5. Adjust screwdriver control on top of P65 amplifier, A1 for d-c balance (±1 mv d-c).

u. Connect oscilloscope to TP2. (Do not remove jumper.) Adjust signal oscillator frequency control for a beat note frequency of 1 1/2 Hz. Measure peak-to-peak voltage. This should be 0.5 ±0.1 V.

v. Connect oscilloscope to TP5. Adjust R2 for a gain of 16. Increase beat note frequency till amplitude at TP5 drops to 0.707. Record frequency. This break due to R24, C23 should be at about 20 Hz.

w. Reconnect signal inputs to J1 and J2 per Steps c, d and e.

7.6 Alignment and Test Procedure for Phase-Lock Loop Filter Module

7.6.1 Test Equipment List

Quan.	Description	Manufacturer	Model #
1	RF Voltmeter	Boonton Electronics	91C
1	Signal Generator	Hewlett Packard	606
1	Vacuum Tube Voltmeter	Hewlett Packard	410B
1	DC Voltage Source 0 to -4 V.		
1	Microvoltmeter	Kay	302B
2	DC Power Supplies	Hewlett Packard	721A
1	620 ohm, 1/2 W. Resistor		

7.6.2 Procedure

7.6.2.1 Signal-to-Noise Detector Section (Q1 - Q7)

Apply +18 VDC to Pin 4 J2 and -18 VDC to Pin 5 J2. Pin 1 is ground. Check for excessive current in either supply lead. Refer to Figure 7-5 for a block diagram of the test set-up and to Figure 8-16 for a schematic diagram of the module.

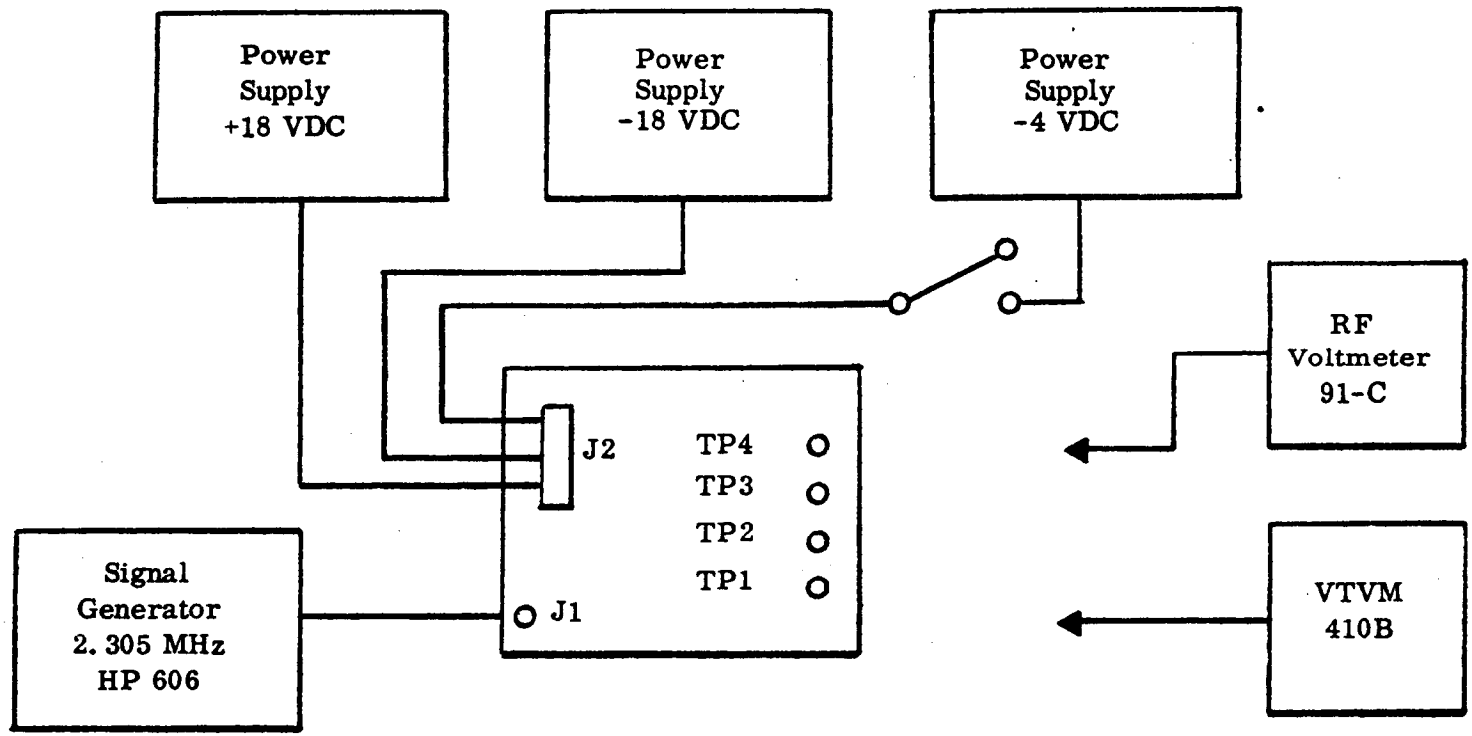


Figure 7-5. PLL Filter Module Test Setup

Apply a 2.305 MHz signal to J1 and adjust T1, T2 and T3 for maximum DC at TP3. Check to see that the output at TP3 is essentially linear with input signal level up to at least 5V DC.

With 5V DC output at TP3, adjust R20 until voltmeter at TP2 changes from 0 to 5 V. (Meter should suddenly change from one reading to the other as R20 is changed.) With R20 set at point where voltmeter at TP2 just changes from 0 to 5 V, reduce 2.305 MHz input to J1 until voltmeter at TP2 changes from 5V to 0 V. This should require less than 2 db reduction in signal level. Reduce 2.305 MHz input to J1 until voltmeter at TP3 reads 0.5 volts. Readjust R20 until voltmeter at TP2 changes from 0 to 5 V. Reduce input to J1 until voltmeter at TP2 changes from 5 V to 0. This should require less than 2 db change in signal at J1.

7.6.2.2 Acquisition Circuit - Loop #1 (Q8 - Q10)

Connect a 100 ohm resistor from Pin 12 of J2 to -18 V supply (Pin 5, J2). Apply a DC voltage source of zero to -4 volts to Pin 3 J2. Read the voltage at TP1 with the HP 410B VTVM. When the input voltage is zero TP1 should show zero volts. When the input falls to -4 V the voltage at TP1 should be +5 V. TP1 can be trimmed to +5 volts by tailoring R39 if necessary. Change voltage to Pin 3, J2. At a voltage of around 1 volt, TP1 should change back to 0 volts, and at about 2 volts, TP1 should change to +5 V. If necessary, tailor R36 to obtain the change within this range.

7.6.2.3 Acquisition Circuit - Loop #2 (Q13 - Q14)

Apply a DC voltage source of zero to -4 volts to Pin 16 J2. Connect a 620 ohm, 1/2 watt resistor between Pin 4 and Pin 17 J2. Measure the voltage across the resistor with the HP 410B VTVM. With zero input volts the resistor voltage should be near zero volts. With the input voltage at -4 the resistor voltage should be at least 17 volts. Resistor current should change rapidly when voltage at Pin 16, J2 is between -1 and -2 volts. If necessary, tailor R58 to obtain this condition.

7.6.2.4 Check Voltage Levels at Zener Diodes

Diode	Voltage
CR-3	-15
CR-4	+15
CR-5	+10
CR-6	-10

7.6.2.5 Check and Alignment of the Phase-Lock Filter and Tuning Circuits

a. Check output range of R67 by observing J2 - 18 and turning R67 to each extreme. The range should be about +9 to -9 volts.

b. Set zero trims, R46 and R64. Energize K1 by applying -4 V to Pin 3, J2. Ground Pin 6, J2. Adjust R46 for zero volts at TP4. Remove -4 V from Pin 3, J2 and open Pin 6, J2. Turn R67 for zero volts at J2 - 18, then ground J2 - 18. Make sure J2 - 6 is open circuited (no input). Place VTVM at TP4. Adjust R64 for zero reading on VTVM. (Use a scale with sensitivity of around 0.1 volts full scale.) Remove ground from J2 - 18.

7.6.2.6 Check of Doppler Polarity and Frequency Analog Outputs

Look at voltage at TP4, J2 - 9 and J2 - 8 with VTVM. Set R67 for the following listed TP4 values and observe the outputs at J2 - 9 and J2 - 8.

TP4	J2 - 9	J2 - 8
Zero	Zero ±0.05 V	+2.5 ±0.5 Volts
+9 Volts	+6 ±1	+4.5 ±.5 Volts
-9 Volts	-6 ±1	+0.5 ±.5 Volts

7.7 Alignment and Test Procedure for VCO-1 Module

Refer to Figure 7-6 for block diagram of test connections.

7.7.1 Test Equipment List

Quan.	Description	Manufacturer	Model #
2	DC Power Supplies	Hewlett Packard	721A
1	RF Voltmeter	Boonton Electronics	91C
1	Oscilloscope	Tektronix	531
1	Spectrum Analyzer	Lavoie	LA19
1	Counter	Hewlett Packard	524B
1	Digital Volt-Ohmeter	Beckman/Berkeley	5350
1	RF Generator	Hewlett Packard	608

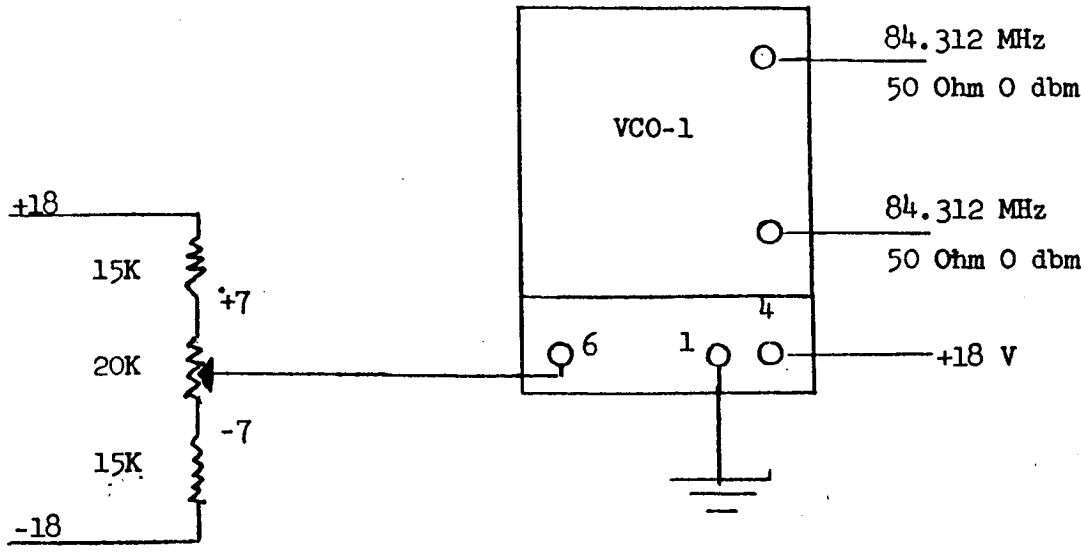


FIGURE 7-6 Block Diagram of VCO-1 Module

7.7.2 Alignment

a. Connect the RF Voltmeter to J2 (50 ohm load). Apply +18 V DC to J1 - 4.

b. Tune L1, L2, T1 and T2 for maximum output at J2.

c. Connect the RF Voltmeter to J3 (50 ohm load).

d. Tune T3 for maximum output at J3.

7.7.3 Test Procedure

a. Connect the RF Voltmeter to J3 (output 0 dbm ±1 db). Connect the RF Voltmeter to J2 (output 0 dbm ±1 db).

b. Connect the Spectrum Analyzer to J2.

c. Check for harmonic components of 10.539 MHz (At least 40 db attenuation except for the desired 84.312 MHz). The output at J3 should be the same as the J2 output.

d. Disconnect the VCXO output.

e. Inject an 84.312 MHz (+10 dbm) signal (RF Generator at J2) through a 10 db attenuator. Connect the spectrum analyzer to J3. The 84.312 MHz signal must be down at least 40 db (-40 dbm) from J2 signal input.

f. Reconnect the VCXO output.

g. Vary the input DC control at J1 - 6. Connect the counter to J3.

h. The output frequency should vary linearly over ±9 volt range at 17.6 KHz/volt.

7.8 Alignment Procedure for Doppler Detector Module

a. Input - 140.52 MHz to J1.

Observe - TP1 using high impedance probe of 91-C

Adjust C2 for maximum capacity.

Adjust C4 for maximum output.

Adjust C2 for maximum output.

Check bandpass characteristics for double peaks. If double peaks or asymetrical characteristic is observed, reduce capacity of C3 by bending "tabs" and repeat this step. "Tabs" are silver plated copper ribbon soldered to top of C2 and C4.

b. Input - 140.52 MHz to J1.

Observe - Base Q2 using high impedance probe of 91-C

Adjust C8 for maximum output.

c. Input - 140.52 MHz to base Q8.

Observe - Emitter Q2 using high impedance probe of 91-C

Adjust C47 for maximum output.

d. Input - 140.52 MHz to base Q7.

Observe - Emitter Q2 using high impedance probe of 91-C.

Connect 1.2 K 1/4 W resistor across L20 and adjust C43 for maximum output.

Remove 1.2 K resistor from L20 and connect across L21 and adjust C41 for maximum output. Remove 1.2 K resistor.

e. Input - 28.104 MHz to base Q6.

Observe - Collector Q7 using high impedance probe of 91-C

Connect 3.3 K 1/4 W resistor across L17 and adjust C37 for maximum output.

Remove 3.3 K resistor from L17 and connect it across L18 and adjust C35 for maximum output. Remove 3.3 K resistor.

f. Input - 14.052 MHz to TP2. (Be sure to use blocking capacitor at this point is not at DC ground.)

Observe - Collector C6 using high impedance probe of 91-C

Adjust C29 for maximum output.

g. Input - 70.26 Mc to J3.

Observe - TP2 using high impedance probe of 91-C.

Adjust C17 to maximum capacity.

Adjust C24 for maximum output.

Adjust C17 for maximum output.

Check pass band. If double peaked or asymetrical, reduce C20 by bending "tabs" apart. If pass band is too narrow increase C20. If C20 is changed repeat this step.

h. Input - 84.312 MHz to J5.

Observe - TP3 using high impedance probe of 91-C

Adjust C21 to maximum capacity.

Adjust C23 for maximum output.

Adjust C21 for maximum output.

Check pass band. If couble peaked or asymetrical, reduce C22 by bending "tabe". If too narrow, increase C22. If C22 is changed, repeat this step.

During the entire alignment procedure it is important to keep the input signal noise level below the point where saturation occurs.

7.9 Alignment and Test VCO-2 Module

7.9.1 Test Equipment List

Quan.	Description	Manufacturer	Model #
2	Transistorized Power Supplies	Power Designs Inc.	Model 5015A (or capable of ±18 V at 150 ma)
1	RF Voltmeter	Boonton Electronics	91-C
1	DC Vacuum Tube Voltmeter	Hewlett Packard	412A
1	Special 2.342 Mc Signal Generator w/Phase Modulator		
2	Attenuator	Kay 30-0	432C
1	Oscilloscope	Tektronixs	531 w/Type B plug-in unit
1	Frequency Counter	Hewlett Packard	524-B w/Video Head
1	Phase Meter	Technology Instrument Corp.	Type 320A
1	Crystal Oscillator 2.342 MHz w/223 MV Output to 50 ohms		

7.9.2 Procedure

a. Apply +18 and -18 volt power to module.

b. Check and record both currents.

c. Check for -15 volts DC at CR1.

d. Check for +15 volts DC at CR2.

e. Check tuning circuit. K1 not energized. Look with DC voltmeters at TP3 and TP4. Turn R3 full cw then full ccw. TP5 should vary to at least +2.5 and -2.5 volts. TP3 should follow TP5.

f. Balance R1 and R2. Set R3 for zero volts at TP5, then ground TP5. Adjust R2 for zero volts at negative input to A2 or TP6. Next adjust R1 for zero volts at TP4. Repeat adjustment procedure for R2 and R1 if necessary. Remove ground from TP5. Final adjustment will be made in receiver alignment.

g. Alignment of Output Amplifiers. Set R3 for zero volts at TP3. With RF voltmeter and 50 ohm load observe level at J2. Tune T1 for maximum output at J2. Output at J2 should be

+10 dbm into a 50 ohm load. If more than 1 db in error, tailor R20. Record level at J2. Check and record level at TP2. Check and record level at J3. Tune T2 for maximum output at J3. This level should be 0 dbm ±1 db. Tailor R27 if necessary. Record level at J3.

h. Check and record voltages at J1 - 14 and at J1 -9 also record frequency at J2 with frequency counter for the following four settings of R3. First set R3 for 2.342000; 2.342500 and 2.341500 MHz on counter. Then set R3 for zero voltage at J1 - 14. Voltage at J1 - 14 should vary over a range of -2.5 to +2.5 volts. Voltage at J1 - 9 should vary over a range of 0 to 5 volts.

7.10 Alignment and Test Procedure for 2.342 MHz Phase Detector Module

7.10.1 Test Equipment List

Quan.	Description	Manufacturer	Model #
2	DC Power Supplies	Hewlett Packard	721A
1	RF Voltmeter	Boonton Electronics	91C
1	DC VTVM	Hewlett Packard	412A
1	Oscilloscope	Tektronix	531
1	Signal Generator	Hewlett Packard	606
	Use 2.342 MHz Reference from Frequency Synthesizer		
2	Attenuator	Kay 30-0	432C

7.10.2 Procedure

a. Remove jumper from TP1 to TP2. Remove jumper from TP3 to TP4. Set R1, C1 and C2 to approximate mechanical center.

b. Apply +18 VDC and +18 VDC to J3.

c. Connect 2.342 MHz reference signal (with attenuator) to J1.

d. Connect RF Voltmeter to J1 (use high impedance probe). Adjust reference input level to 230 mv RMS.

e. Connect 2.342 MHz signal generator (with attenuator) to J2. Connect RF Voltmeter and adjust signal input level to 7 mv RMS.

f. Connect oscilloscope to TP1 and adjust signal generator frequency control to approximately 100 cps either side of 2.342 MHz. (Observe 100 Hz beat note on scope.)

g. Tune T4 and T3 for maximum beat note amplitude.

h. Decrease reference signal input until beat note amplitude is approximately 1/10 the value observed after completion of Step g.

i. Tune T1 and T2 for maximum beat note amplitude (it may be necessary to repeat Step h. several times while tuning T1 and T2 for maximum).

j. Repeat Step d.

k. Connect oscilloscope to TP4 and adjust T5 for maximum beat note amplitude.

l. Decrease reference signal input until beat note amplitude is approximately 1/10 the value observed after completion of Step k.

m. Tune T6 for maximum beat note amplitude. (It may be necessary to repeat Step l. several times while tuning T6.)

n. Repeat Steps c, d, and e.

o. Connect oscilloscope to TP4. Adjust 2.342 MHz signal input level (7 mv RMS ±0.5 mv RMS) until the beat note amplitude at TP4 is equal to 0.5 volt p-p. (0.25 V/Rad). Tailor R14 if necessary.

p. Connect DC Voltmeter to TP4. Adjust C2 for DC balance (±1 mv DC). (Tailor R44 if necessary to obtain the required balance.) (R44 may be in series with R30, R31, R32 or R33 as required.)

q. Disconnect signals from J1 and J2.

r. Connect jumper from TP1 to TP2.

s. Connect DC Voltmeter to TP4. Adjust screwdriver control on top of P65 amplifier, A1 for DC balance (±1 mv DC).

t. Reconnect signal inputs to J1 and J2 per Steps c, d and e.

u. Connect oscilloscope to TP2. (Do not remove jumper.) Adjust signal oscillator frequency control for a beat note frequency of 1 1/2 Hz. Measure peak-to-peak voltage. This should be 0.5 ±0.1 V.

v. Connect oscilloscope to TP5. Adjust R2 for a gain of 16. Increase beat note frequency till amplitude at TP4 drops to 0.707. Record frequency. This break due to R24, C23 should be at about 20 Hz.

w. Connect jumper from TP3 to TP4.

x. Look at TP1 with oscilloscope (jumper in) and obtain a 1 KHz beat note. Record amplitude. Check and record amplitude of 1 KHz output at J4, with R11 set for maximum.

y. Adjust R11 for 5 V. p-p output at J4 at 1 KHz. Increase beat note frequency and observe frequency at which output drops by 3 db (to 3.5 volts). This should be in the order of 100 KHz or higher.

7.11 Alignment and Test Procedure for Range Signal Extraction Module

7.11.1

Quan.	Description	Manufacturer	Model #
1	Vacuum Tube Voltmeter	Hewlett Packard	410B
1	DC Oscilloscope	Hewlett Packard	150A
1	Signal Generator	Hewlett Packard	606A
2	Signal Generators	Hewlett Packard	200C
2	Power Supplies	Hewlett Packard	721A
2	500 ohm Load Resistance		
2	1 K 1/2 Watt Resistors		
1	Frequency Counter	Hewlett Packard	524C
1	Video Amplifier	Hewlett Packard	526A

7.11.2 Procedure

73.18 KHz Channel (Q1 - Q3)

Apply ±18 VDC to Pins 4 and 5 of J2, respectively. Pin 1 is ground. Check for excessive current in either supply lead. Refer to Figure 7-7 for a block diagram of the test set-up and to Figure 8-21 for a schematic of the module.

Apply a 73.1875 KHz signal to J1 at 0.5 V peak-to-peak, 500 ohms. With the two bandpass filters connected properly, adjust R10 to obtain a 707 millivolt RMS sine wave (2 V p-p) at J6 (TP2) across a 500 ohm load.

1 KHz Video Extraction Channel (Q4 - Q7)

Modulate the 73.1875 KHz signal at J1 with a 1 KHz square wave. Adjust R19 about mid-range. Connect a DC oscilloscope to J7 (TP3)

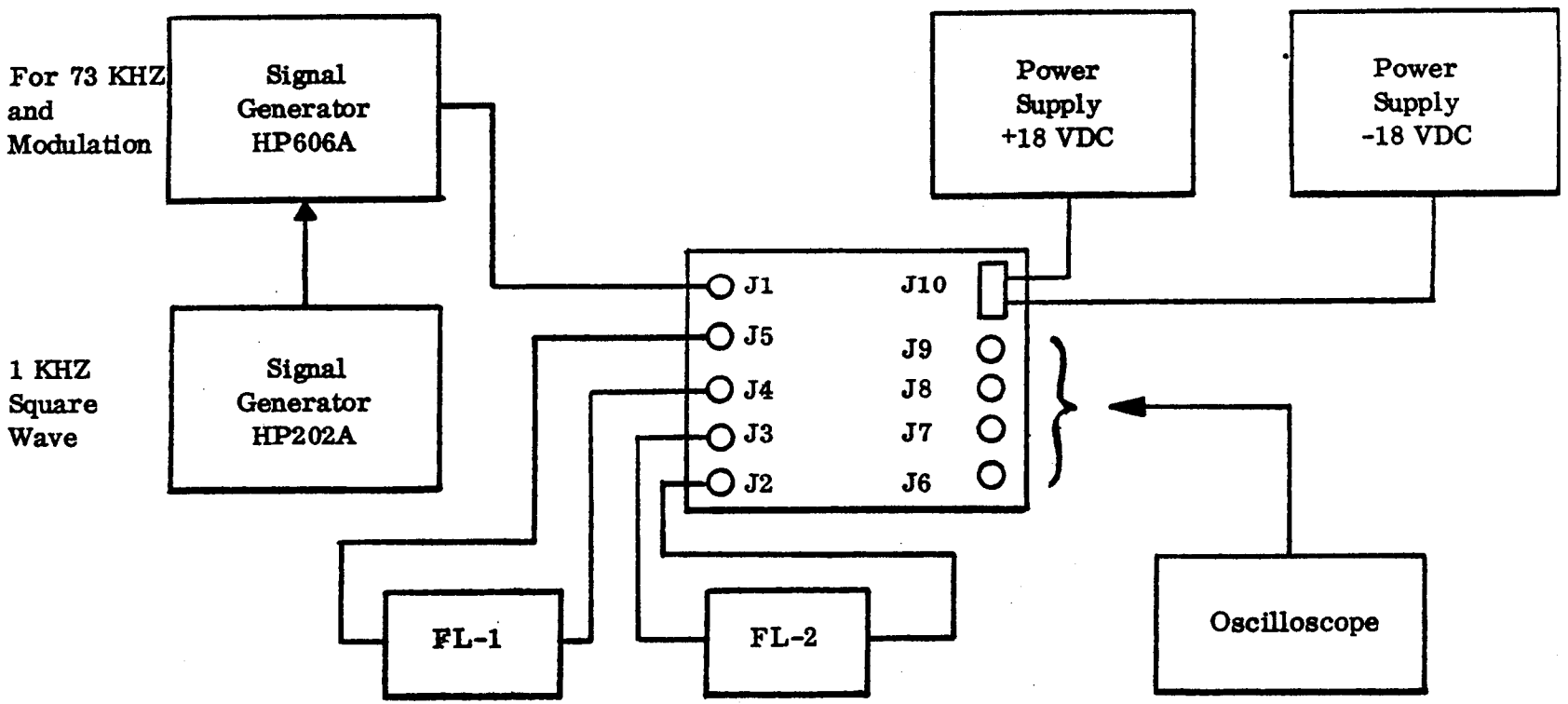


Figure 7-7. Test Setup Diagram for Checkout of 73.1875 KHZ and Video Channels

and adjust R31 (clipper adjust) and R34 (level adjust) to obtain a 5.5 volt peak-to-peak square wave which is zero volts at the bottom of each negative going swing. Adjust R31 to provide best balance between positive and negative portions of wave form. J7 should be terminated in 500 ohms for this test. TP3 is located on the printed board.

2.2871 KHz Range Tone Channel (Q8 - Q13)

Apply a 2.2871 KHz signal at -2 dbm to J1. Monitor the output at J8 (TP5) across 500 ohms with the oscilloscope while adjusting R51, R52, R62, and R63 for maximum output with no oscillation. Then adjust R66 for approximately 0.707 volts RMS. Check the -3 db bandwidth to make certain it is approximately 100 Hz. R103 and R104 might have to be adjusted slightly to set the loop gain in each of the two cascaded amplifiers so that oscillations can be suppressed.

71.47 Hz Range Tone Channel (Q8, Q14 - Q18)

Apply a 71.47 Hz signal at -2 dbm to J1. Monitor the output at J9 (TP6) across 500 ohms with the oscilloscope while adjusting R74, R75, R85, and R86, for maximum output with no oscillation. Then adjust R89 for approximately 0.707 volts RMS. Next apply two signals at J1 at the frequencies 1.108 and 1.179 KHz and each at the same level which produces combined amplitude of 3.1 V p-p at J1 as shown in Figure 7-8. Then 1 K resistors provide isolation between generators. Adjust R66 and R89 for 0.707 volts RMS each at J8 and J9, respectively. Check the output frequency of each channel at TP5 and TP6 for 2.2871 KHz and 71.47 Hz, respectively.

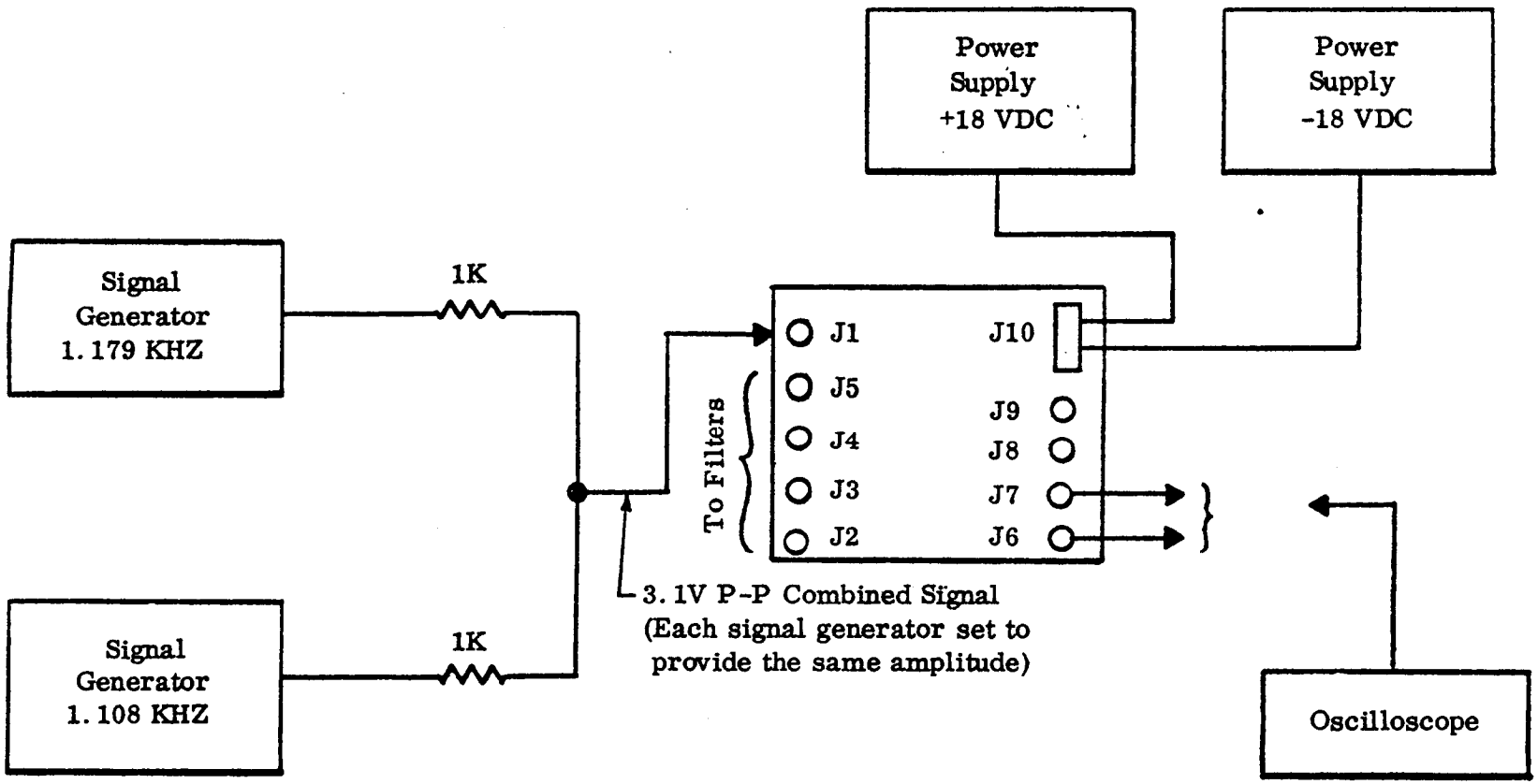
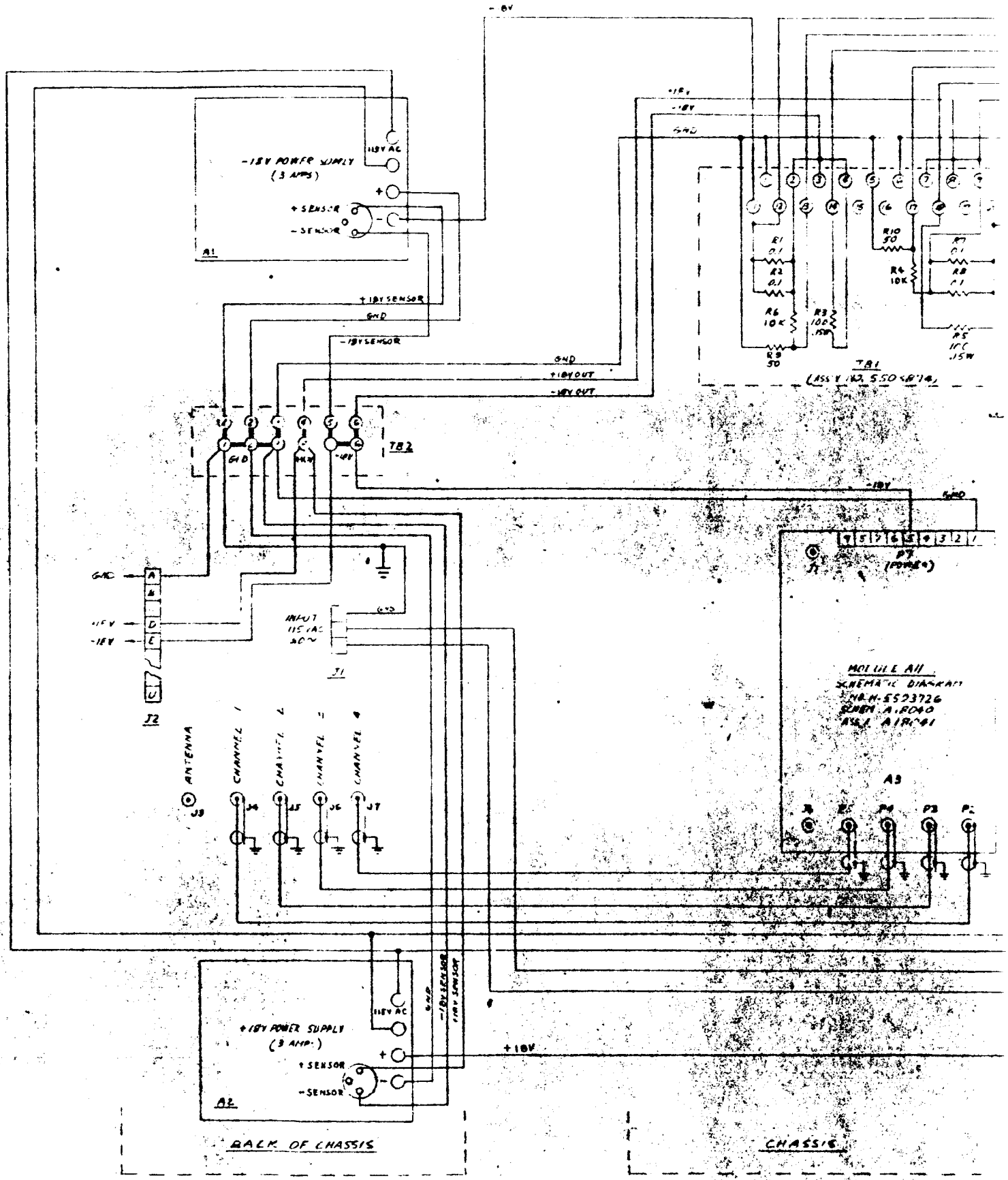


Figure 7-8. Test Setup Diagram for Checkout of 71.47 HZ and 2.2871 KHZ Channels

8.0 SCHEMATICS

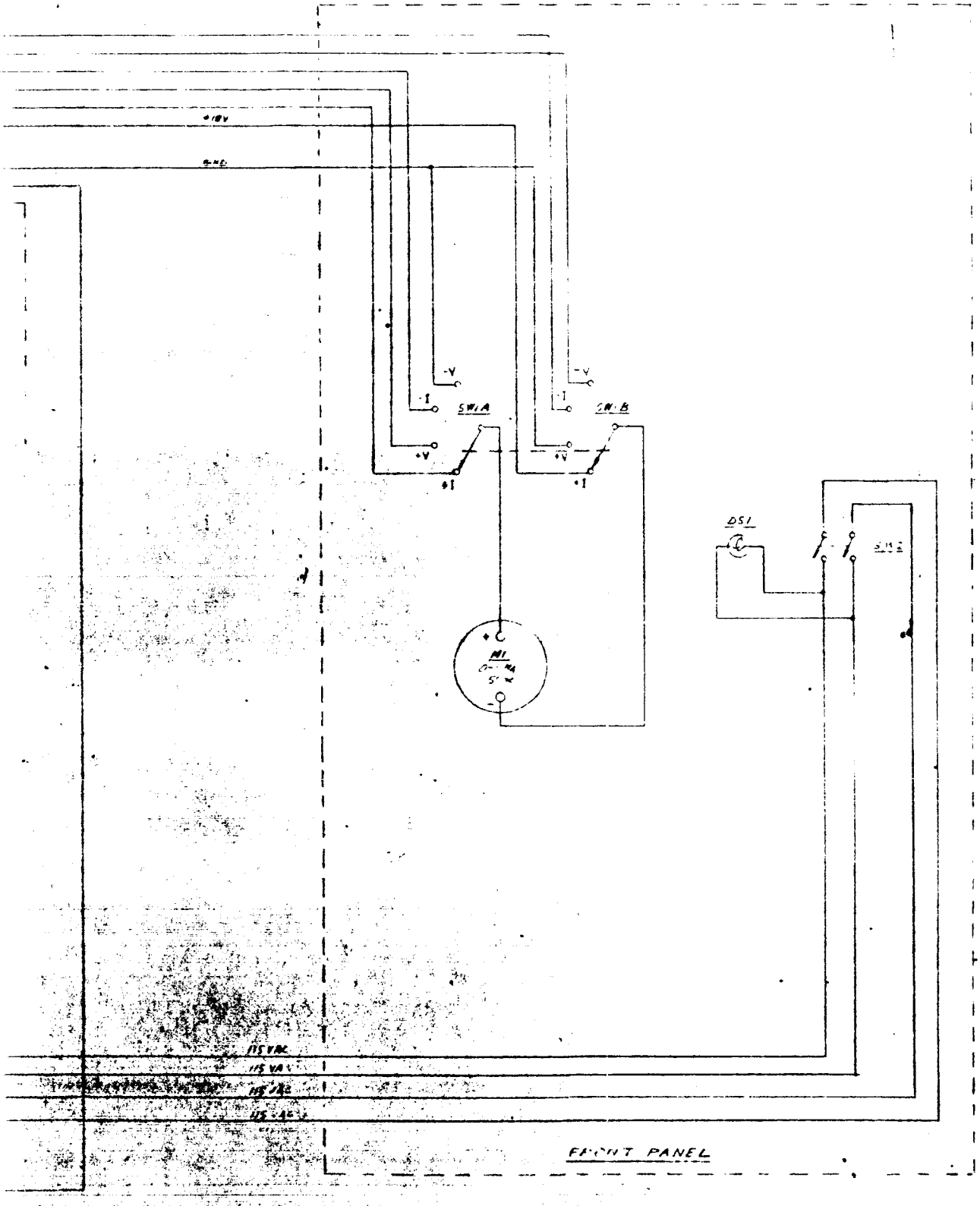
The following are schematic diagrams of the various chassis and modules of the AROD Vehicle Tracking Receiver:

ITTFL #	AROD #	DESCRIPTION	FIGURE #
5503851	A18100	RF and Power Supply Chassis	8-1
5503726	A18040	1st I-F Amplifier	8-2
5504060	A18200	Chassis Schematic - Arod Channel #1	8-3
5504060	A18400	Chassis Schematic - Arod Channel #2	8-4
5504064	A18600	Chassis Schematic - Arod Channel #3	8-5
5504061	A18210	2nd Mixer - Arod Channel #1	8-6
4707224	A18410	2nd Mixer - Arod Channel #2	8-7
5504065	A18610	2nd Mixer - Arod Channel #3	8-8
5504062	A18220	2nd I-F Amplifier - Arod Channel #1	8-9
4707206	A18420	2nd I-F Amplifier - Arod Channel #2	8-10
5504066	A18620	2nd I-F Amplifier - Arod Channel #3	8-11
5504063	A18230	3rd Mixer - Arod Channel #1	8-12
5503725	A18430	3rd Mixer - Arod Channel #2	8-13
5504067	A18630	3rd Mixer - Arod Channel #3	8-14
5503764	A18440	4.684 MHz Phase Detector	8-15
5503788	A18450	PLL Filter	8-16
4707243	A18460	VCO-1	8-17
5503881	A18500	Doppler Detector	8-18
4707251	A18480	VCO-2	8-19
5503790	A18470	2.342 MHz Phase Detector	8-20
5503782	A18490	Range Tone Extraction	8-21



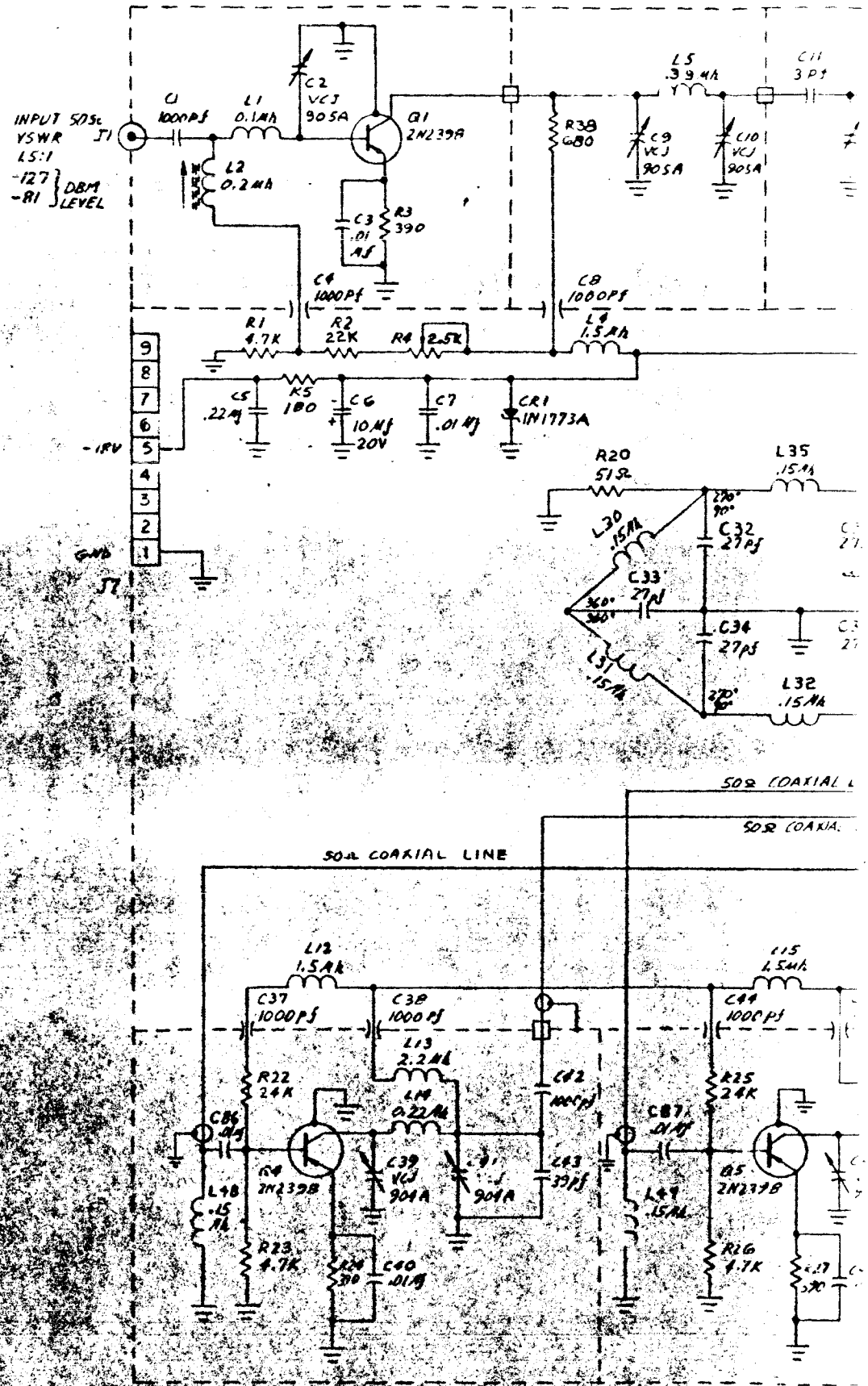
NOTES; UNLESS OTHERWISE SPECIFIED,
1. ALL RESISTANCE VALUES ARE IN OHMS.
(K=1000 M=1000000) 1/2W, 1%

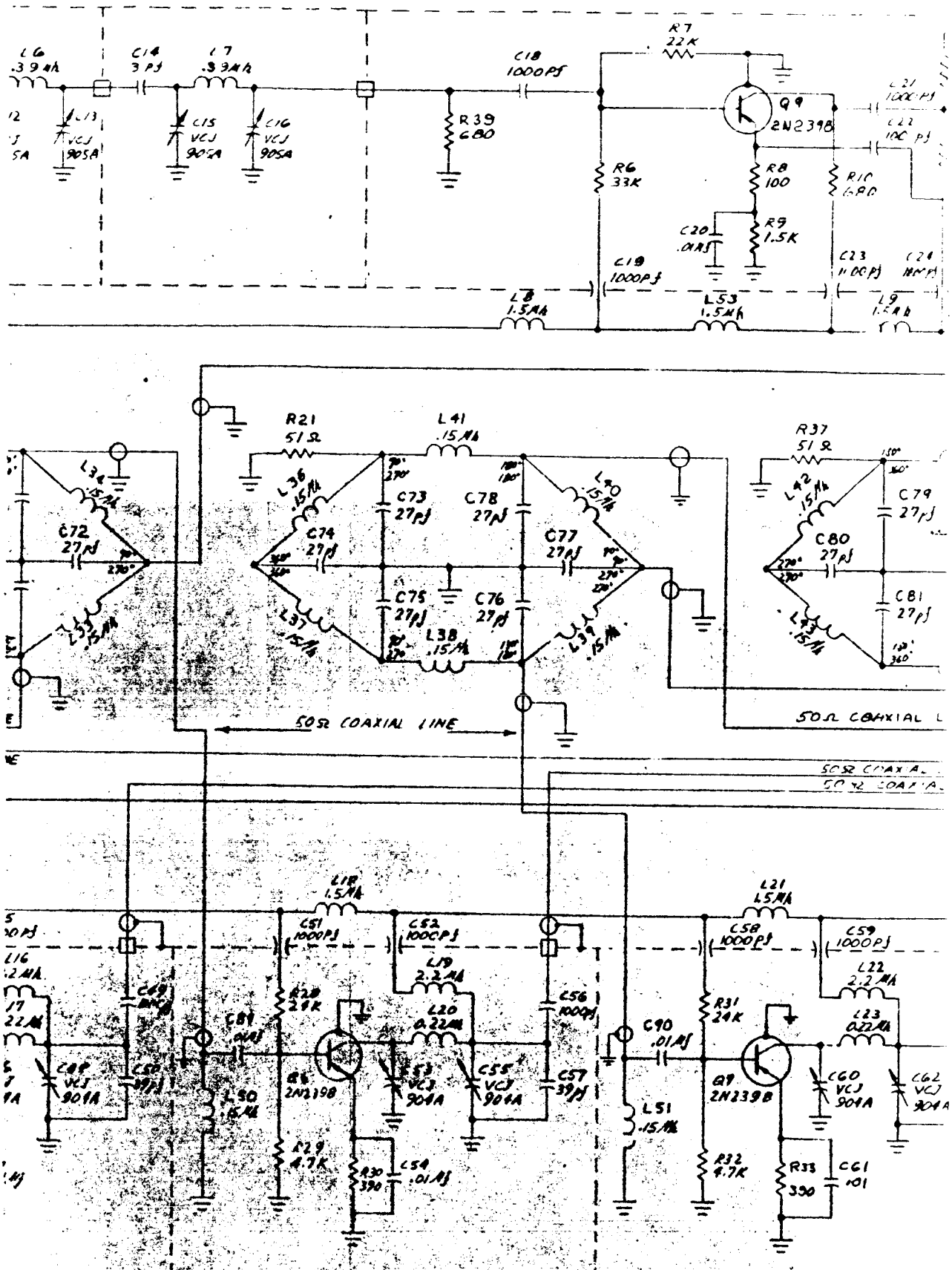
FIG. 8-1 SCHE



, R F AND POWER SUPPLY CHASSIS A 18100

INPUT FREQUENCY TABLE		
CHANNEL	Ø LOCK FREQ	MODULATION FREQ
1	96.9588 MHZ	98.6168 MHZ
2	98.364 MHZ	96.022 MHZ
3	103.7506 MHZ	101.4086 MHZ
4	105.1558 MHZ	102.82 MHZ





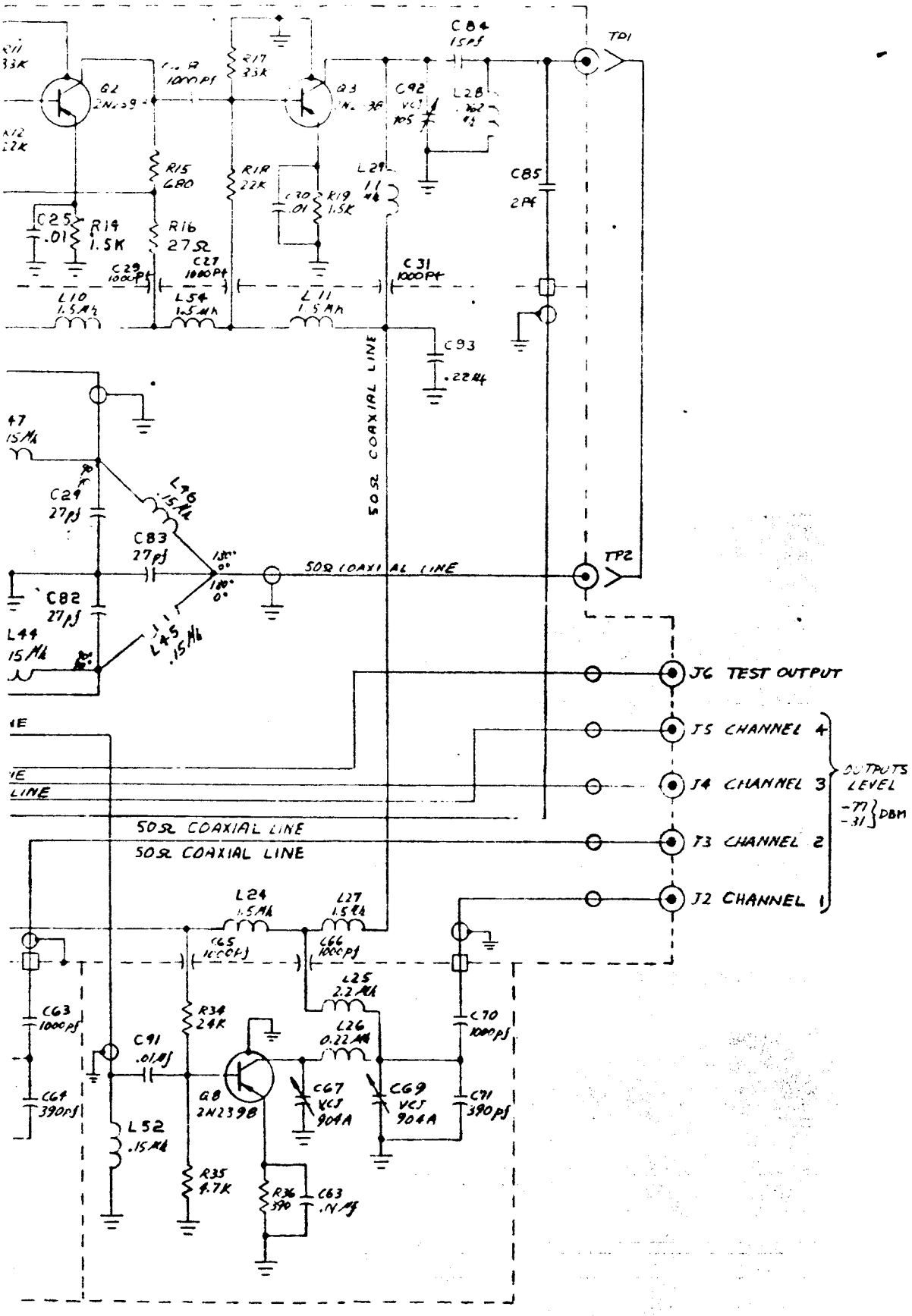
LAST NUMBERS USED

R39	C93	L54
CR1	Q9	J7

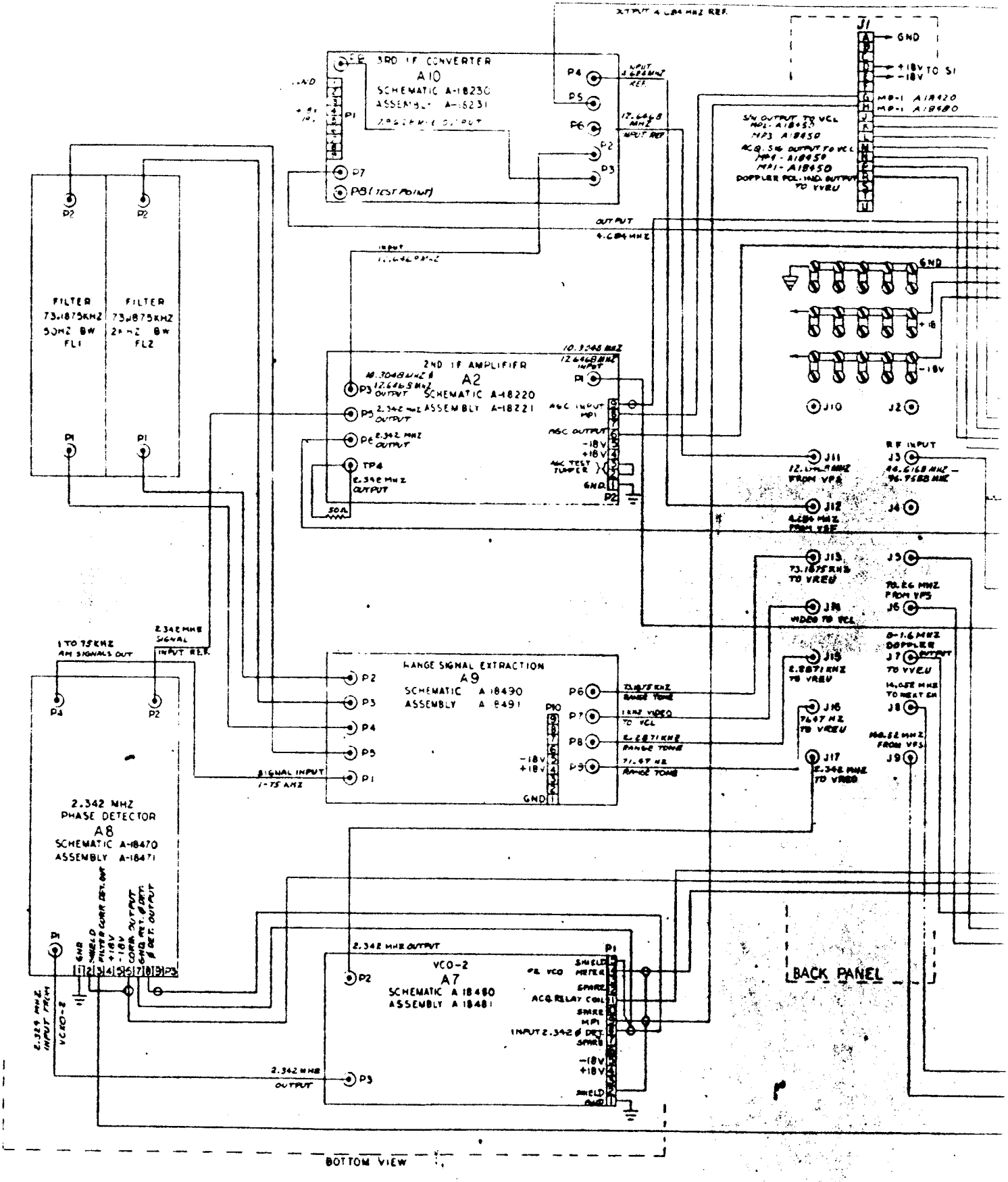
NUMBERS NOT USED

L3 C17

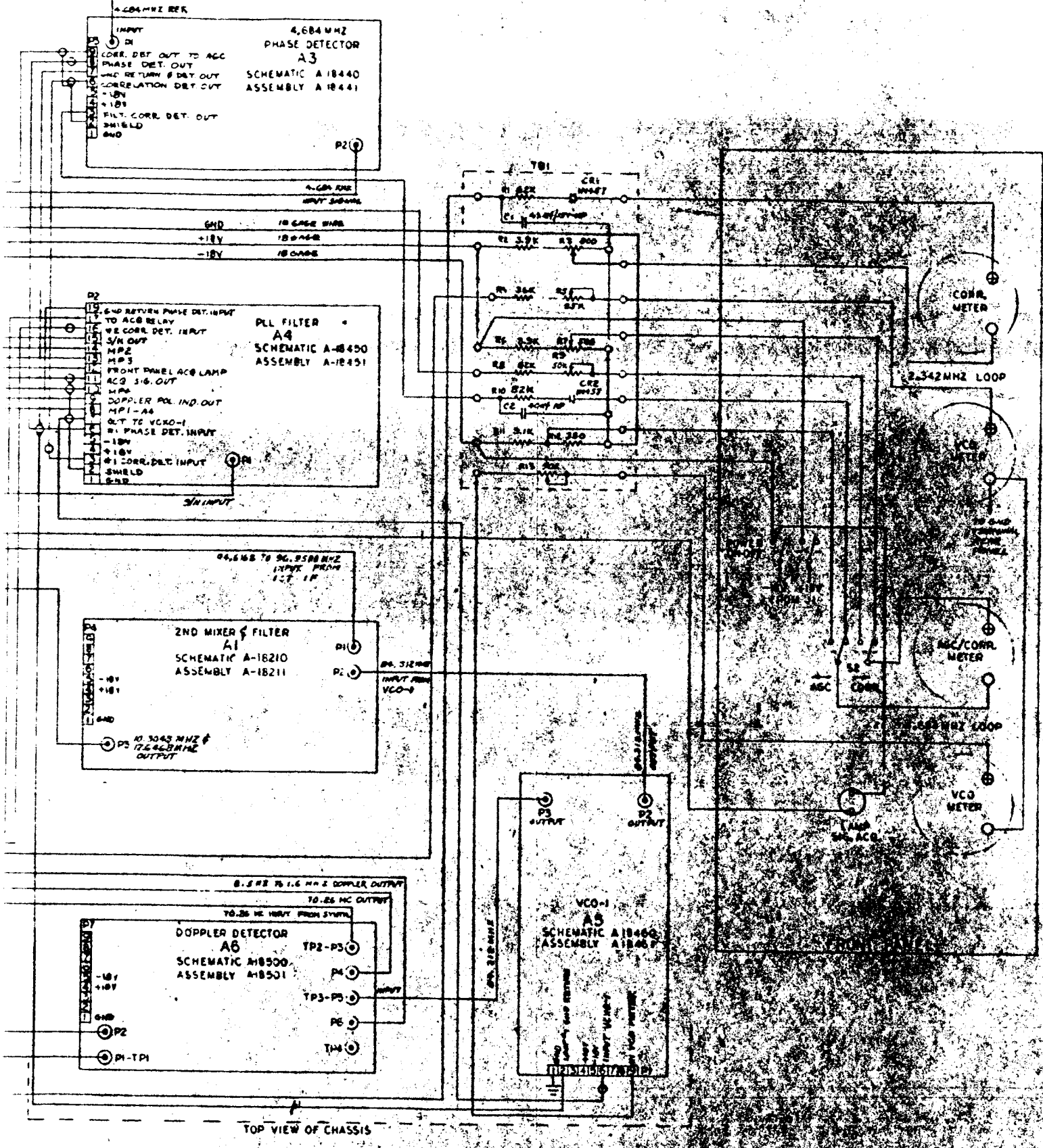
FIG. 8-2 SCHEM.,



ST I F AMPLIFIER A18040


3RD IF CONVERTER
A10
SCHEMATIC A-18230
ASSEMBLY A-18231
FILTER
73.1875KHZ
50HZ BW
FL1
FILTER
73.1875KHZ
2KHZ BW
FL2
2ND IF AMPLIFIER
A2
SCHEMATIC A-18220
ASSEMBLY A-18221
RANGE SIGNAL EXTRACTION
A9
SCHEMATIC A 18490
ASSEMBLY A 8491
2.342 MHZ
PHASE DETECTOR
A8
SCHEMATIC A-18470
ASSEMBLY A-18471
VCO-2
A7
SCHEMATIC A 18480
ASSEMBLY A 18481
BACK PANEL
BOTTOM VIEW

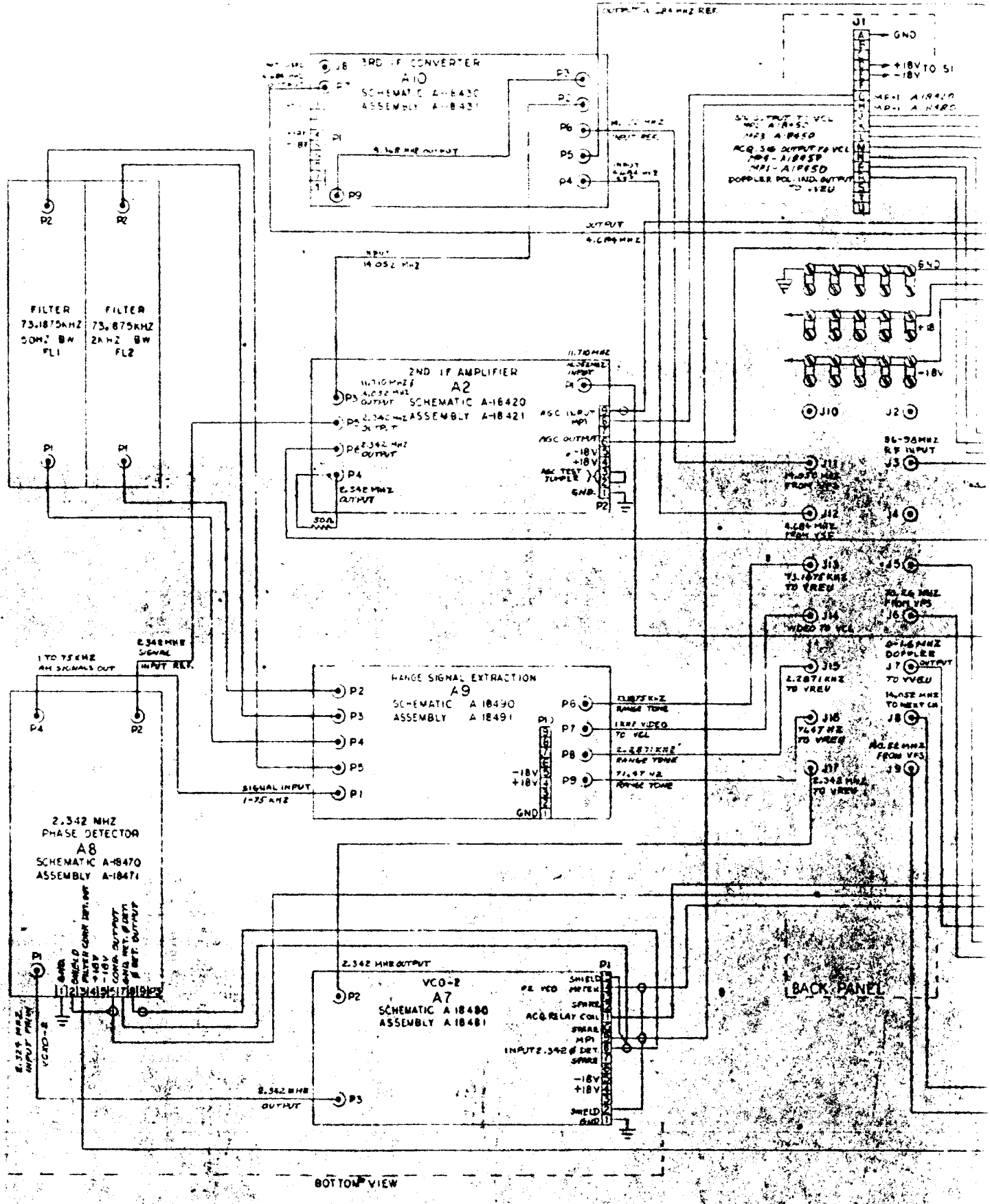
FIG

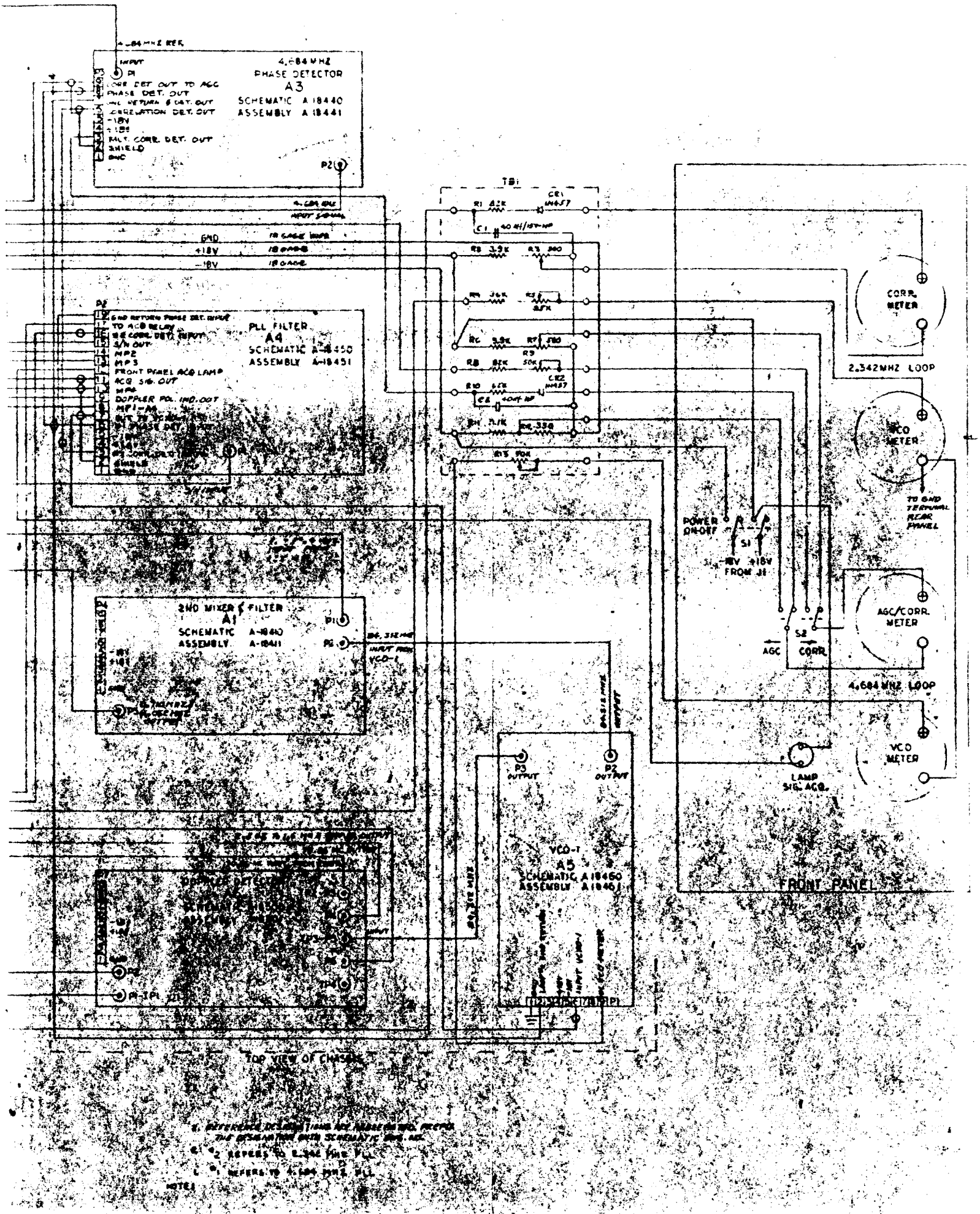


NOTES:

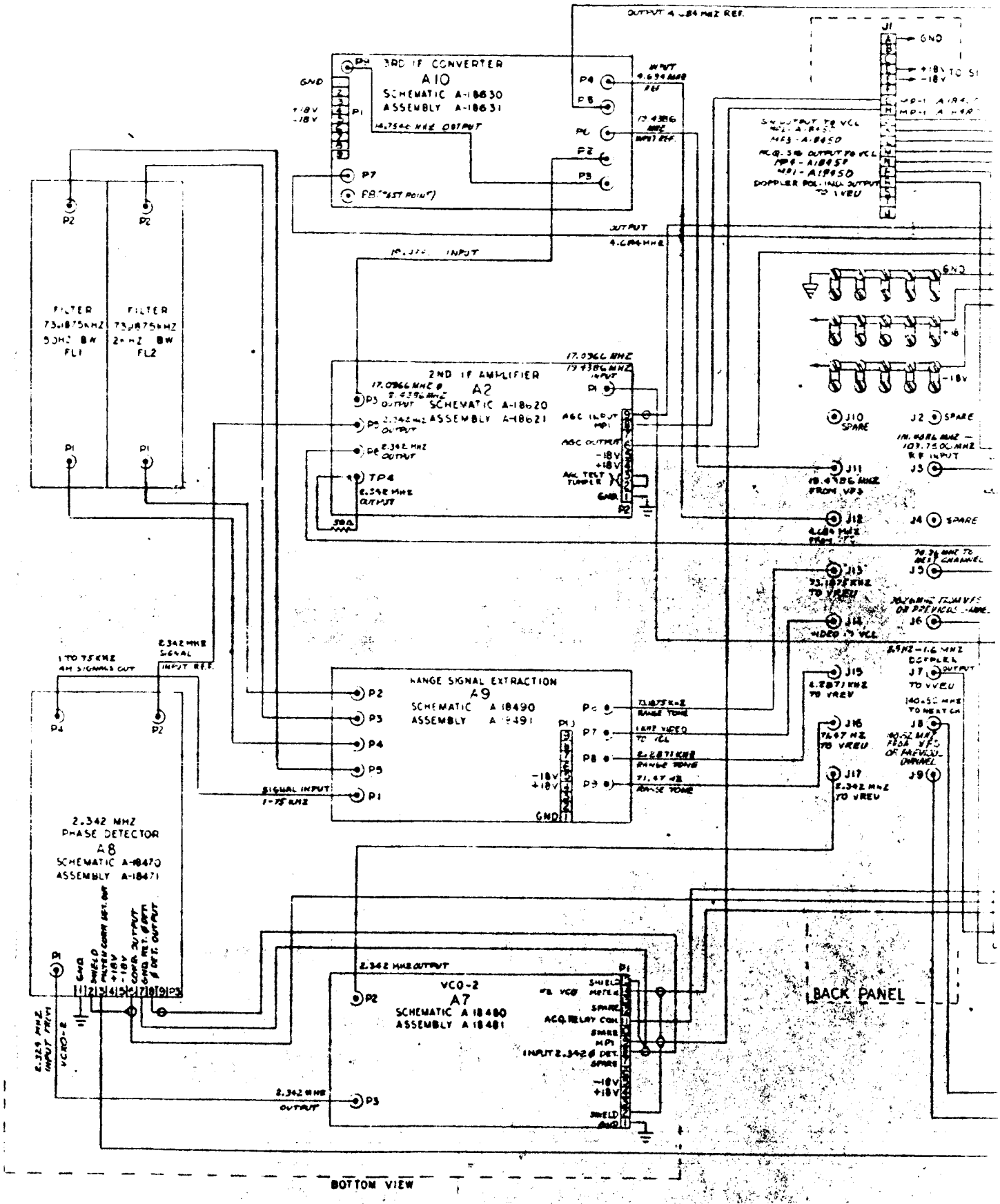
1. REFERENCE DESIGNATIONS ARE ABBREVIATED. PREFIX THE DESIGNATION WITH SCHEMATIC DWG. NO.
2. "2" REFERS TO 2.342 MHZ PLL
3. "1" REFERS TO 4.684 MHZ PLL

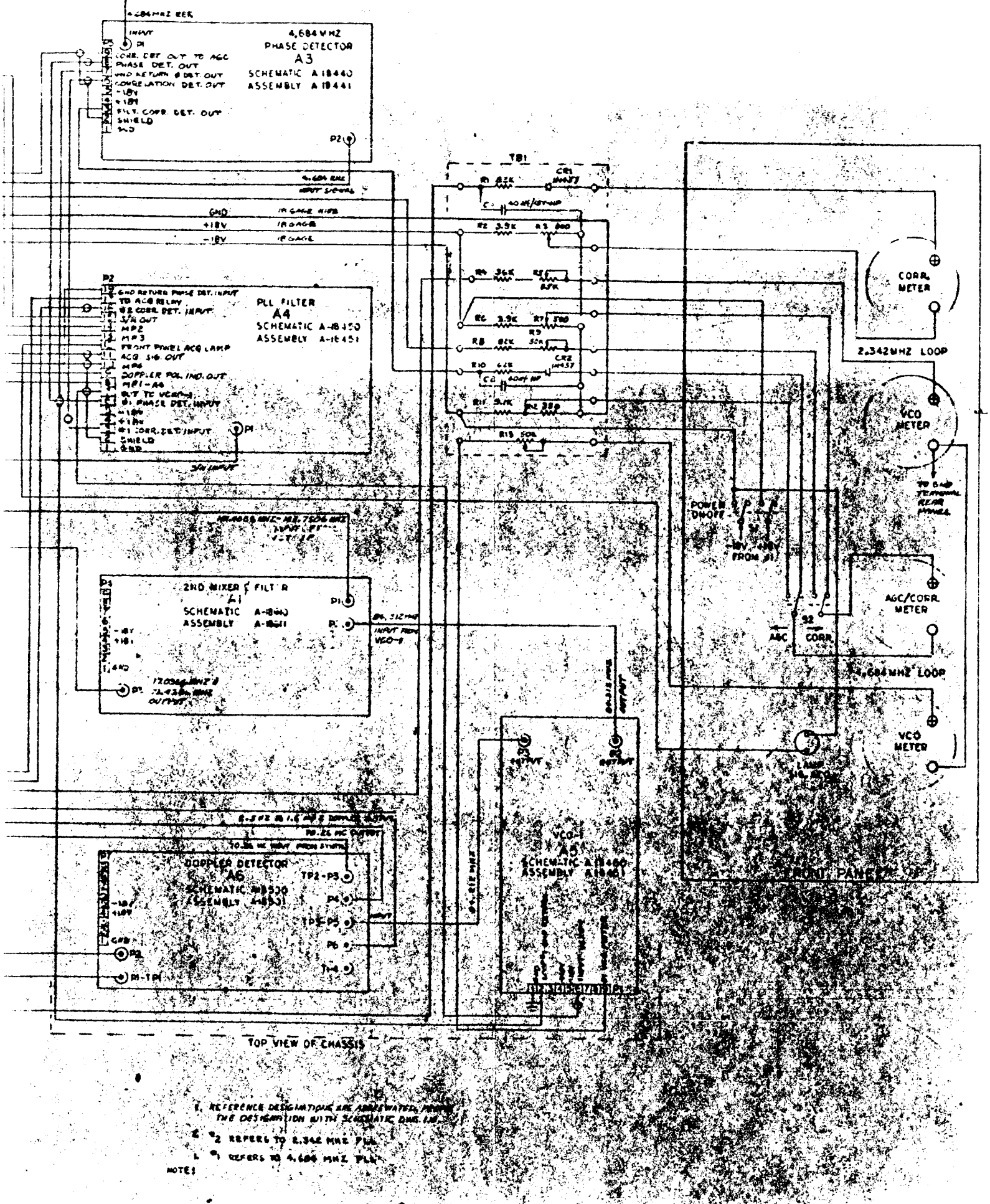
8-3 SCHEM., CHASSIS—AROD CHANNEL NO. 1 A18200


3RD IF CONVERTER
A10
SCHEMATIC A-18430
ASSEMBLY A-18431
FILTER
73.1875KHZ
50HZ BW
FL1
FILTER
73.875KHZ
2KHZ BW
FL2
2ND IF AMPLIFIER
A2
SCHEMATIC A-18420
ASSEMBLY A-18421
RANGE SIGNAL EXTRACTION
A9
SCHEMATIC A 18490
ASSEMBLY A 18491
2.342 MHZ
PHASE DETECTOR
A8
SCHEMATIC A-18470
ASSEMBLY A-18471
VCO-2
A7
SCHEMATIC A 18480
ASSEMBLY A 18481
BACK PANEL
BOTTOM VIEW
GND
+18V TO SI
-18V
J1
J10
J2
J3
J4
J5
J6
J7
J8
J9
J11
J12
J13
J14
J15
J16
J17
P1
P2
P3
P4
P5
P6
P7
P8
P9

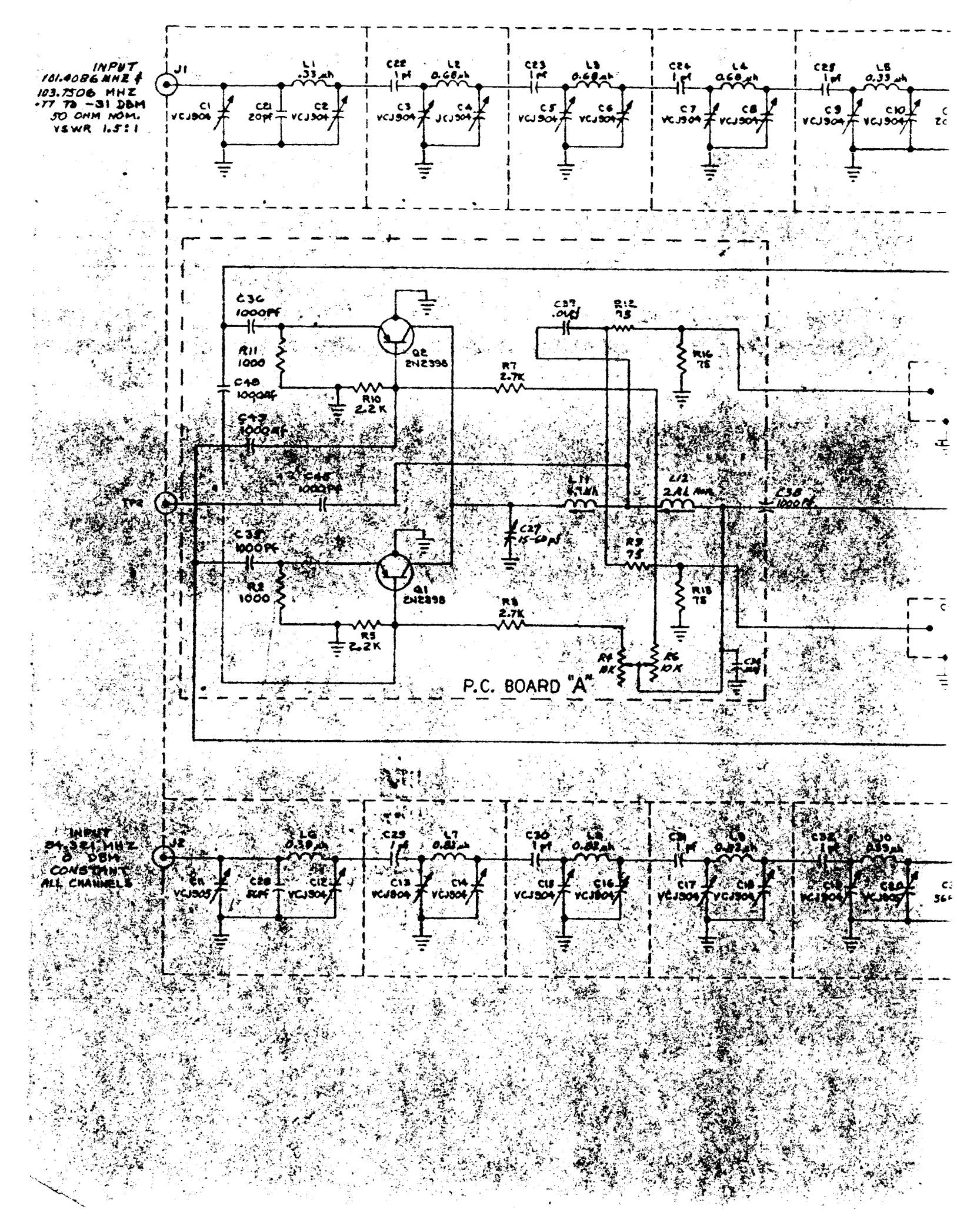


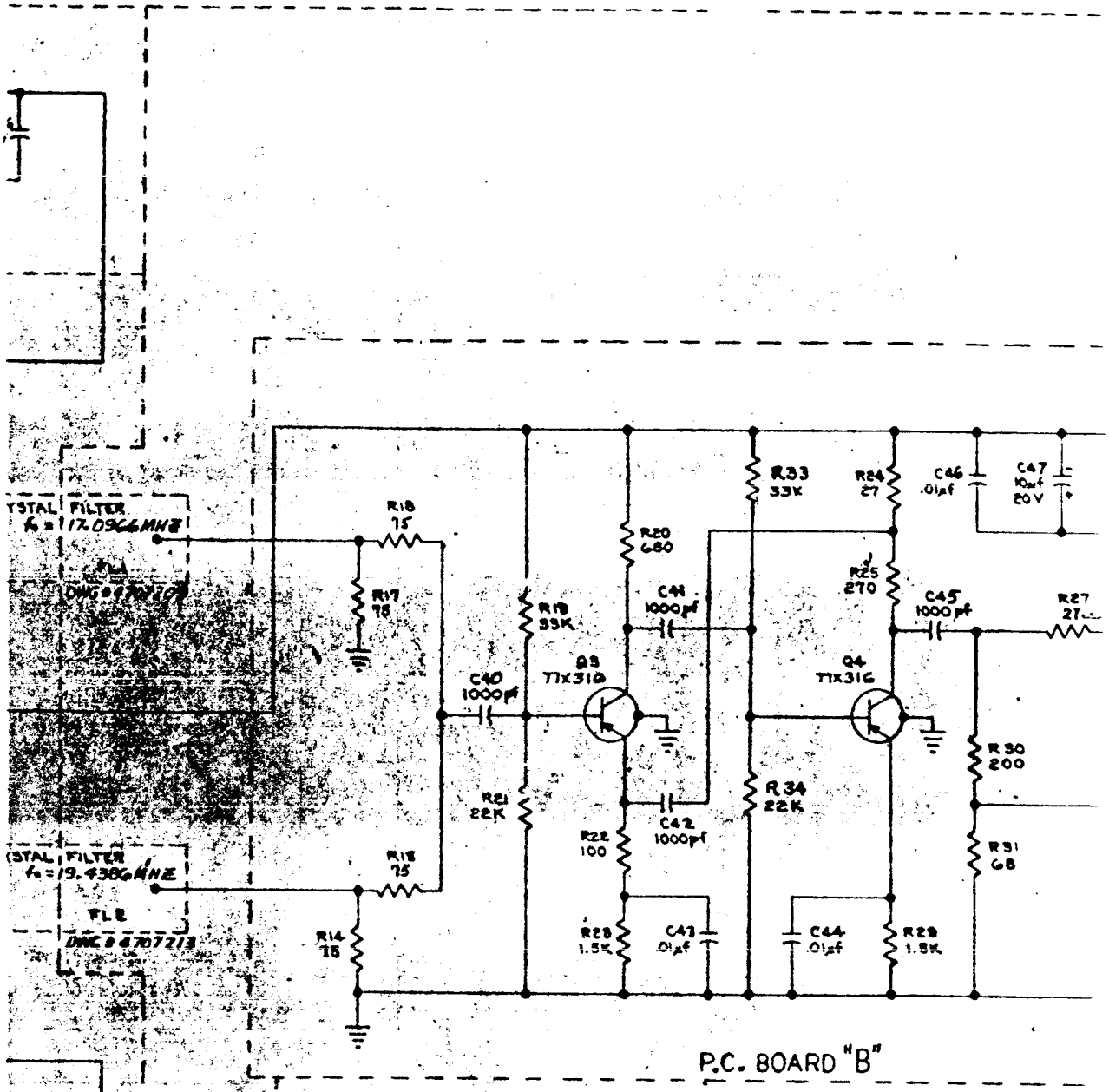
8-4 SCHEM., CHASSIS – AROD CHANNEL NO. 2 A18400


3RD IF CONVERTER
A10
SCHEMATIC A-18630
ASSEMBLY A-18631
FILTER
73.1875KHZ
50HZ BW
FL1
FILTER
73.1875KHZ
2KHZ BW
FL2
2ND IF AMPLIFIER
A2
SCHEMATIC A-18620
ASSEMBLY A-18621
RANGE SIGNAL EXTRACTION
A9
SCHEMATIC A 18490
ASSEMBLY A 18491
2.342 MHZ
PHASE DETECTOR
A8
SCHEMATIC A-18470
ASSEMBLY A-18471
VCO-2
A7
SCHEMATIC A 18480
ASSEMBLY A 18481
BACK PANEL
BOTTOM VIEW



5. 8-5 SCHEM., CHASSIS – AROD CHANNEL NO. 3 A18600

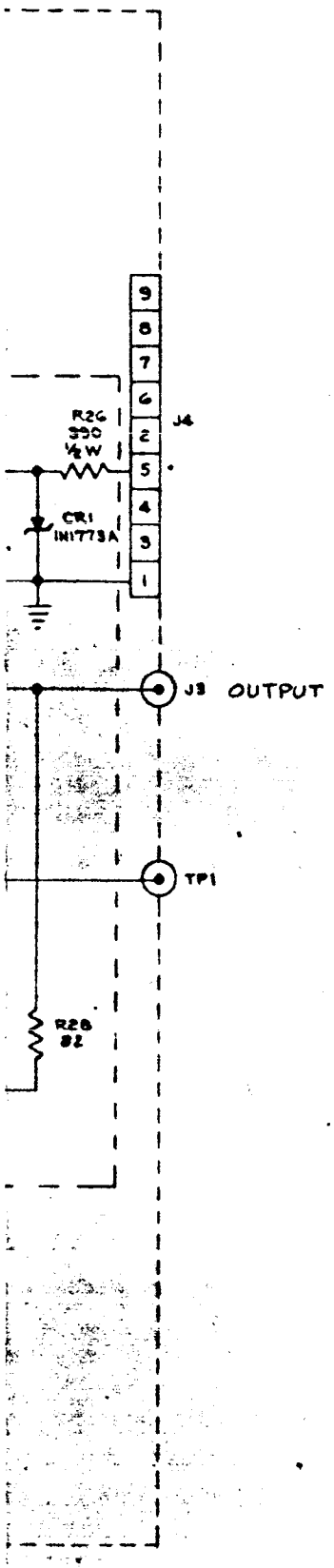

INPUT
101.4086 MHZ &
103.7506 MHZ
-77 TO -31 DBM
50 OHM NOM.
VSWR 1.5:1
J1
L1 .33 μh
C22 1 pf
L2 0.68 μh
C23 1 pf
L3 0.68 μh
C24 1 pf
L4 0.68 μh
C25 1 pf
L5 0.33 μh
C1 VCJ904
C21 20pf
C2 VCJ904
C3 VCJ904
C4 VCJ904
C5 VCJ904
C6 VCJ904
C7 VCJ904
C8 VCJ904
C9 VCJ904
C10 VCJ904
C36 1000PF
R11 1000
C48 1000PF
Q2 2N2398
R10 2.2K
C37 .01μf
R12 75
R16 75
R7 2.7K
C47 1000PF
C45 1000PF
TP2
L11 4.7μh
L12 2.2 μh
C38 1000PF
C27 15-60 pf
C35 1000PF
R2 1000
Q1 2N2398
R5 2.2K
R9 75
R15 75
R8 2.7K
R4 10K
R6 10K
C26 .01μf
P.C. BOARD "A"
INPUT
24.321 MHZ
0 DBM
CONSTANT
ALL CHANNELS
J2
L6 0.39 μh
C29 1 pf
L7 0.82 μh
C30 1 pf
L8 0.82 μh
C31 1 pf
L9 0.82 μh
C32 1 pf
L10 0.39 μh
C11 VCJ905
C28 82pf
C12 VCJ904
C13 VCJ904
C14 VCJ904
C15 VCJ904
C16 VCJ904
C17 VCJ904
C18 VCJ904
C19 VCJ904
C20 VCJ904



LAST NUMBERS USED
L12, Q4, C49, R34
J4, TP2, CR1, FL2

NUMBERS NOT USED
C39, R9, R10, R11, R32

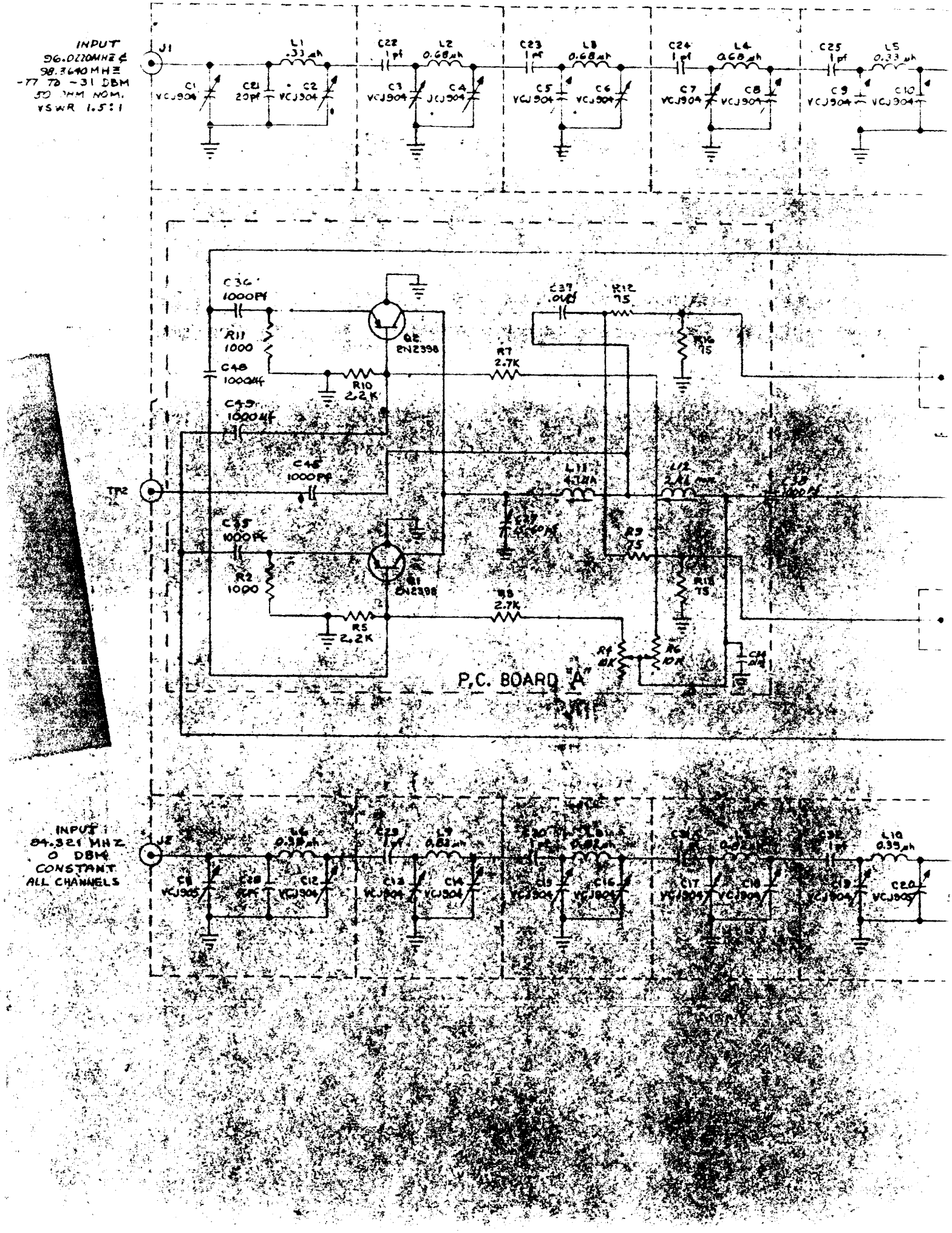
FIG. 8-6 SCHEM



NOTES - UNLESS OTHERWISE SPECIFIED
1. ALL RESISTANCE VALUES ARE IN OHMS ±5%, ½ WATT, INSULATED CARBON.
2. K INDICATES THOUSAND OHMS.

REFERENCE DESIGNATIONS ARE ABBREVIATED
PREFIX THE DESIGNATIONS WITH
SCHEMATIC DWG. NUMBER

2ND MIXER – AROD CHANNEL NO. 1 AIR210


INPUT
96.0220MHz &
98.3640MHz
-77 TO -31 DBM
50 OHM NOM.
VSWR 1.5:1
J1
L1 .33 μh
C22 1 pf
L2 0.68 μh
C23 1 pf
L3 0.68 μh
C24 1 pf
L4 0.68 μh
C25 1 pf
L5 0.33 μh
C1 VCJ904
C21 20pf
C2 VCJ904
C3 VCJ904
C4 VCJ904
C5 VCJ904
C6 VCJ904
C7 VCJ904
C8 VCJ904
C9 VCJ904
C10 VCJ904
C36 1000Pf
R11 1000
C40 1000pf
Q2 2N2398
R10 2.2K
R7 2.7K
C37 .01μf
R12 75
R16 75
C39 1000pf
R9 75
R18 75
C34 .01μf
R4 10K
R6 10K
C41 10μf
C43 1000pf
C42 1000pf
TP2
C38 1000pf
L11 4.7μh
L12 2.2μh
C35 1000pf
R2 1000
Q1 2N2398
R8 2.7K
R5 2.2K
P.C. BOARD "A"
INPUT
84.321 MHz
0 DBM
CONSTANT
ALL CHANNELS
J2
L6 0.39 μh
L7 0.82 μh
L8 0.82 μh
L9 0.82 μh
L10 0.39 μh
C11 VCJ905
C28 82pf
C12 VCJ904
C13 VCJ904
C14 VCJ904
C15 VCJ904
C16 VCJ904
C17 VCJ904
C18 VCJ904
C19 VCJ904
C20 VCJ904

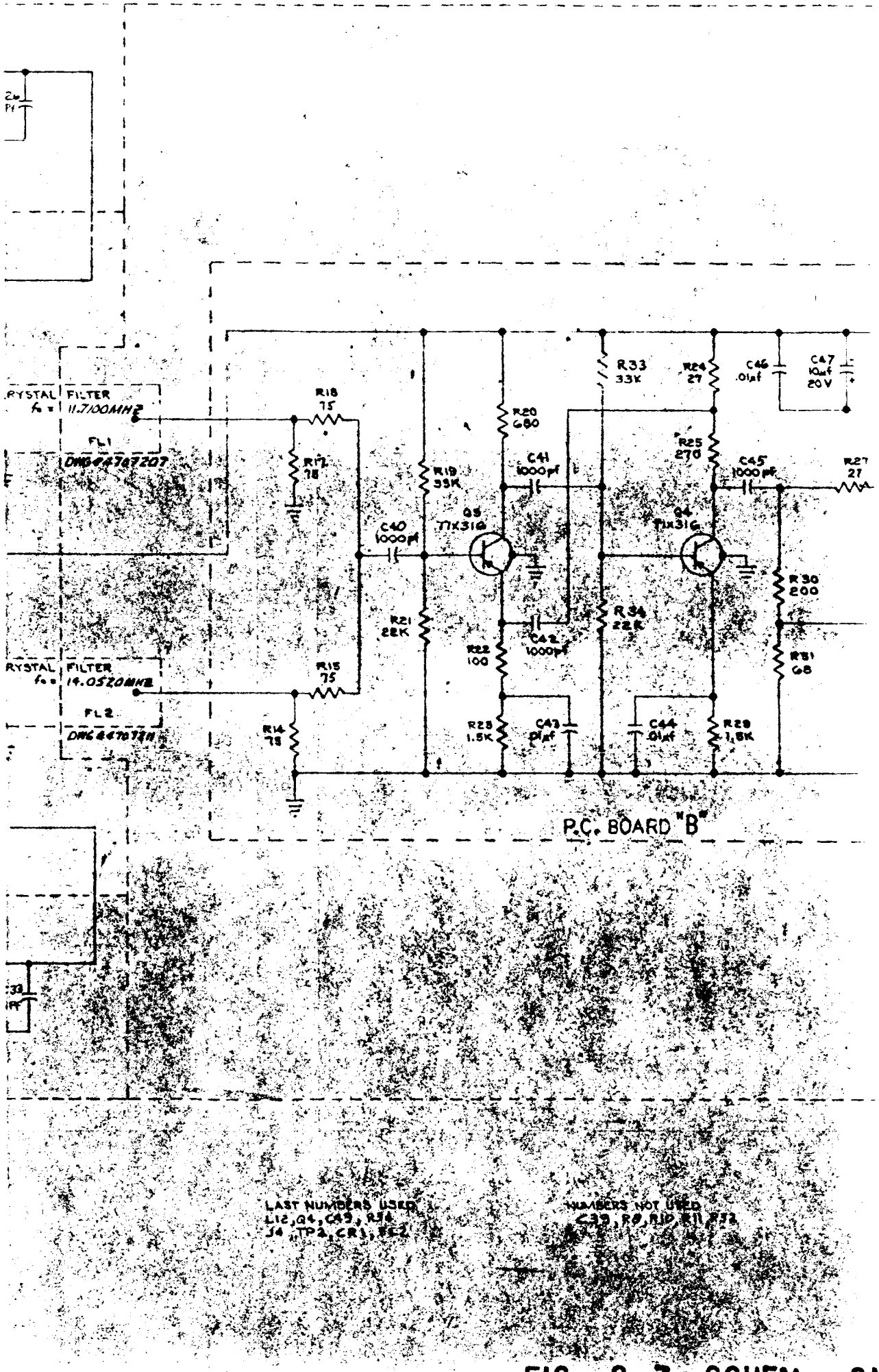
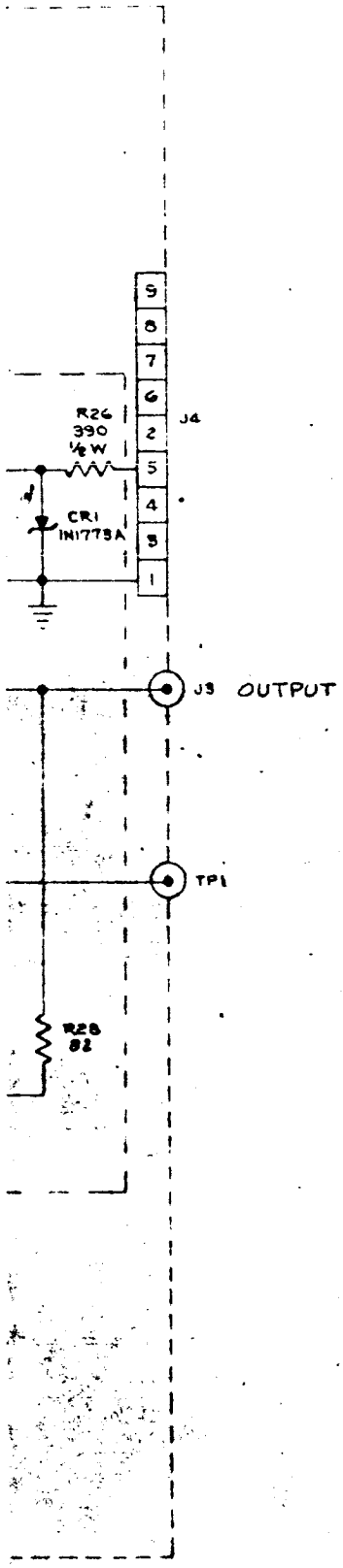


FIG. 8-7 SCHEM., 21

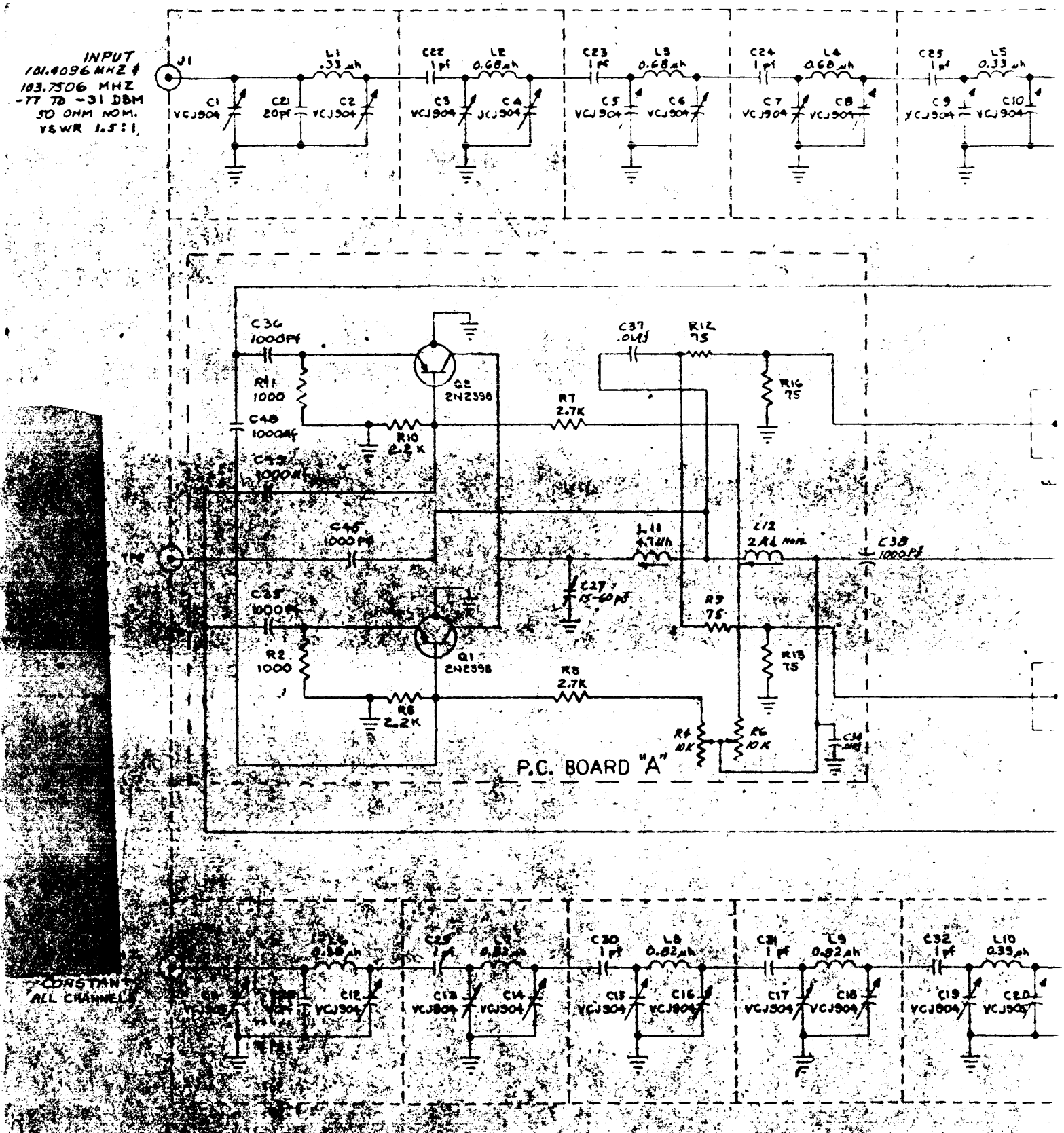


NOTES - UNLESS OTHERWISE SPECIFIED

1. ALL RESISTANCE VALUES ARE IN OHMS ±5%, ¼ WATT, INSULATED CARBON.
2. K INDICATES THOUSAND OHMS.

REFERENCE DESIGNATIONS ARE ABBREVIATED
PREFIX THE DESIGNATIONS WITH
SCHEMATIC DWG. NUMBER

D MIXER – AROD CHANNEL NO. 2 A18410


INPUT
101.4096 MHZ &
103.7506 MHZ
-77 TO -31 DBM
50 OHM NOM.
VSWR 1.5:1
J1
L1 .33 µh
C22 1 pf
L2 0.68 µh
C23 1 pf
L3 0.68 µh
C24 1 pf
L4 0.68 µh
C25 1 pf
L5 0.33 µh
C1 VCJ804
C21 20pf
C2 VCJ504
C3 VCJ904
C4 VCJ504
C5 VCJ504
C6 VCJ504
C7 VCJ504
C8 VCJ504
C9 VCJ504
C10 VCJ504
C36 1000PF
C37 .01µf
R12 75
R16 75
Q2 2N2398
R11 1000
R7 2.7K
C40 1000pf
R10 2.2 K
C41 1000pf
C45 1000 PF
L11 4.7µh
L12 2.2µ h nom.
C38 1000pf
TP1
C27 15-60 pf
C35 1000 PF
R9 75
R13 75
Q1 2N2398
R2 1000
R8 2.7K
R6 2.2K
R4 10K
R5 10K
C34 .01µf
P.C. BOARD "A"
L6 0.56 µh
C25 1 pf
L7 0.82 µh
C30 1 pf
L8 0.82 µh
C31 1 pf
L9 0.82 µh
C32 1 pf
L10 0.39 µh
C11 VCJ504
C12 VCJ504
C13 VCJ804
C14 VCJ504
C15 VCJ504
C16 VCJ804
C17 VCJ504
C18 VCJ504
C19 VCJ804
C20 VCJ804
CONSTANT ALL CHANNELS

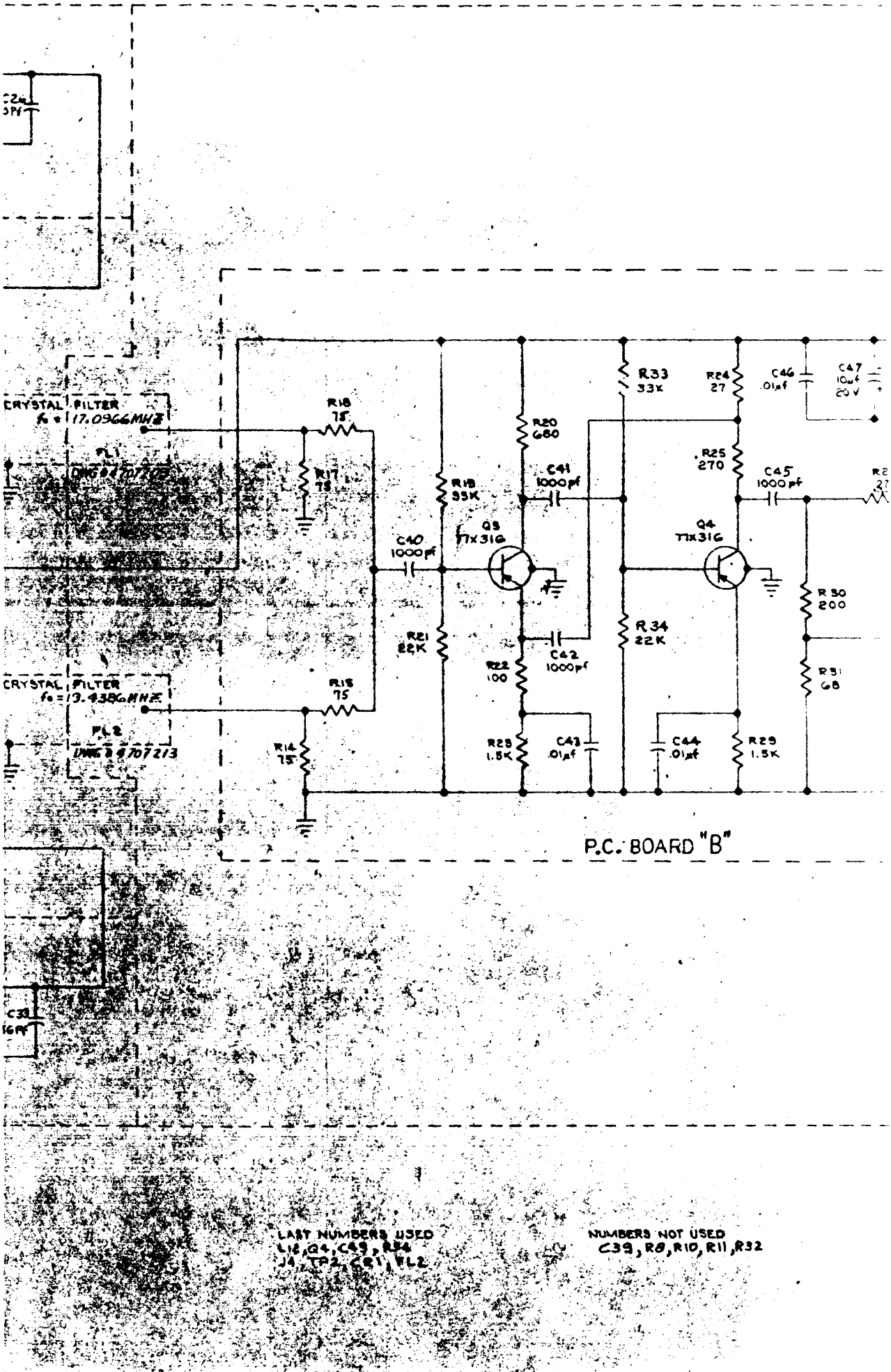
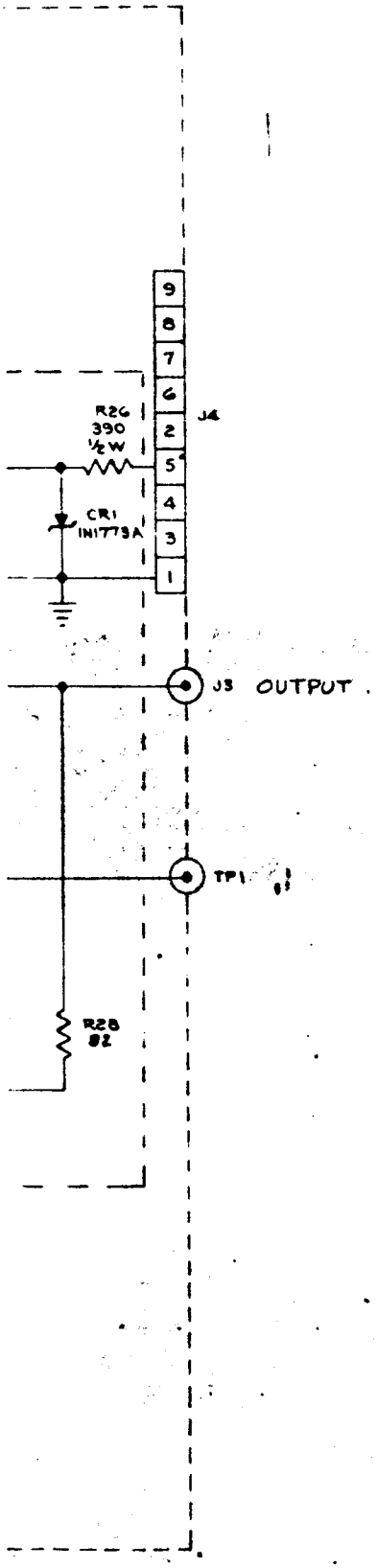


FIG. 8-8 SCHEM., 2ND

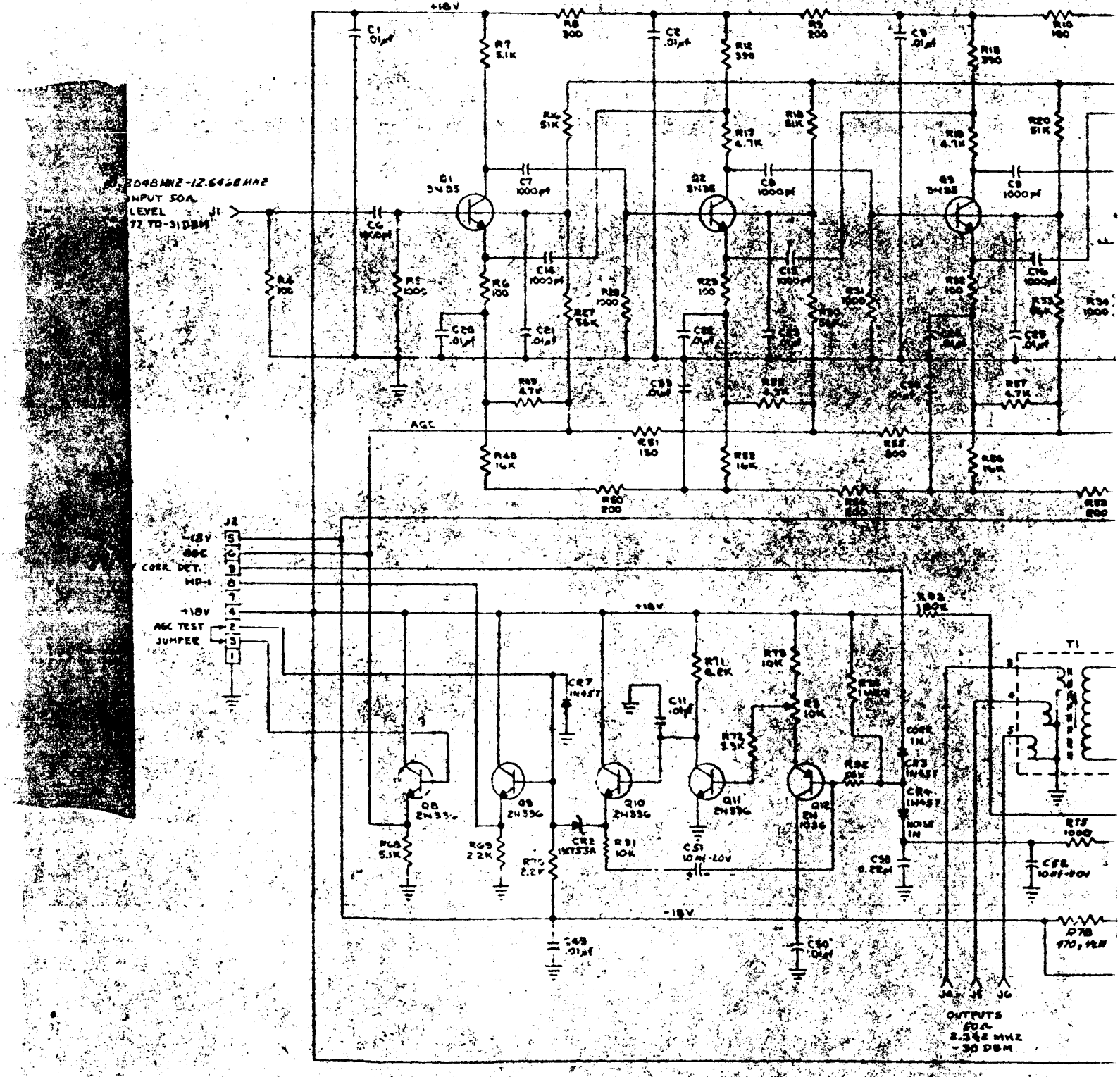


NOTES - UNLESS OTHERWISE SPECIFIED

1. ALL RESISTANCE VALUES ARE IN OHMS ±5%, ½ WATT, INSULATED CARBON.
2. K INDICATES THOUSAND OHMS.

REFERENCE DESIGNATIONS ARE ABBREVIATED PREFIX THE DESIGNATIONS WITH *SCHEMATIC DWG. NUMBER*

MIXER—AROD CHANNEL NO. 3


+18V
INPUT 50Ω
LEVEL
77 TO -31 DBM
J1
AGC
J2
-18V
AGC
COMP. DET.
MP-1
+18V
AGC TEST
JUMPER
Q1 2N85
Q2 2N36
Q3 2N85
Q8 2N396
Q9 2N396
Q10 2N396
Q11 2N396
Q12 2N1036
CR7 1N457
CR2 1N753A
T1
OUTPUTS
50Ω
2.342 MHz
-30 DBM

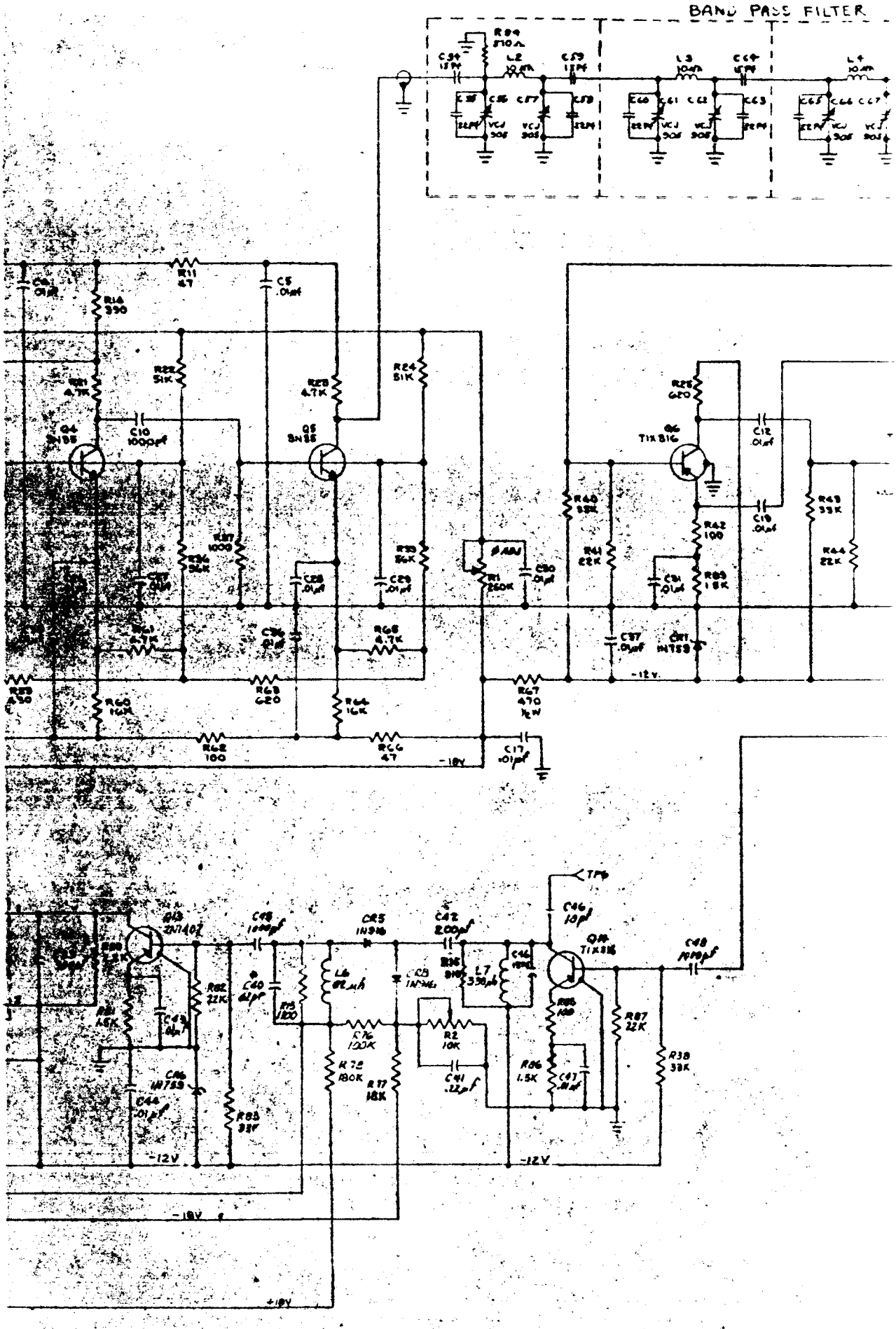
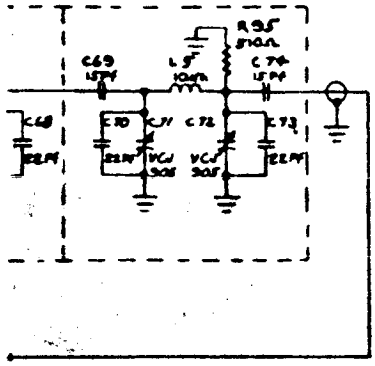
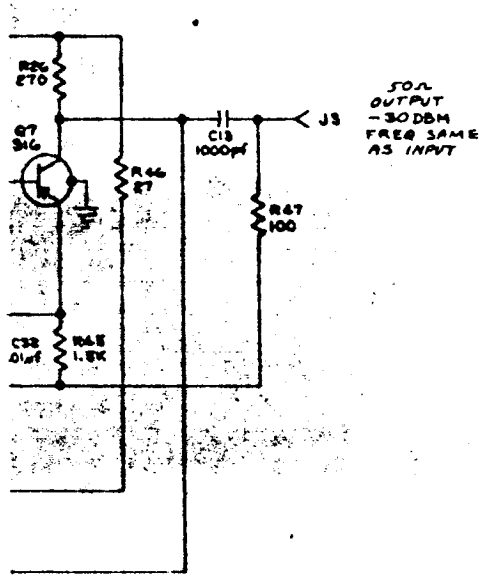


FIG. 8-9 SCHEM., 2ND I F





NOTES - UNLESS OTHERWISE SPECIFIED:
1. ALL RESISTANCE VALUES ARE IN OHMS ±5%, ½ WATT, INSULATED CARBON.
2. K INDICATES THOUSAND OHMS.
3. ✱ SELECT C40 VALUE FOR RESONANCE AT 2.242 MHZ

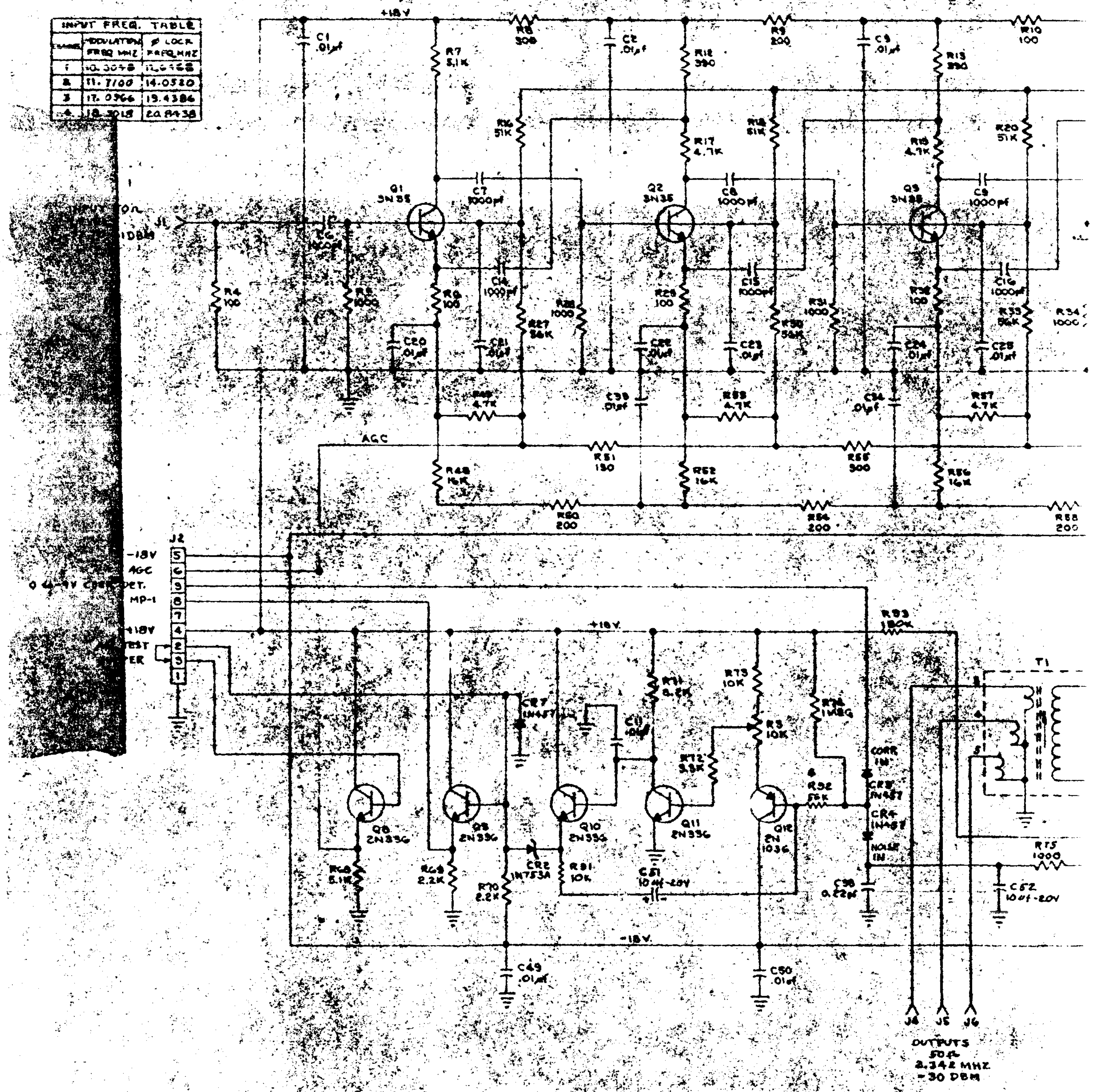
LAST NUMBERS USED
R95 J8 C74 Q14
CR8 L7 T1

NUMBERS NOT USED
C18 L1
R38
R90
R79
R84
R88

REFERENCE DESIGNATIONS ARE ABBREVIATED
PREFIX THE DESIGNATION WITH SCHEMATIC DWG NO

AMPLIFIER - AROD CHANNEL NO. 1 A18220

INPUT FREQ. TABLE		
[illegible]	MODULATION FREQ MHZ	∅ LOCK FREQ MHZ
1	10.3048	12.6468
2	11.7100	14.0520
3	17.0966	19.4386
4	18.3018	20.8438



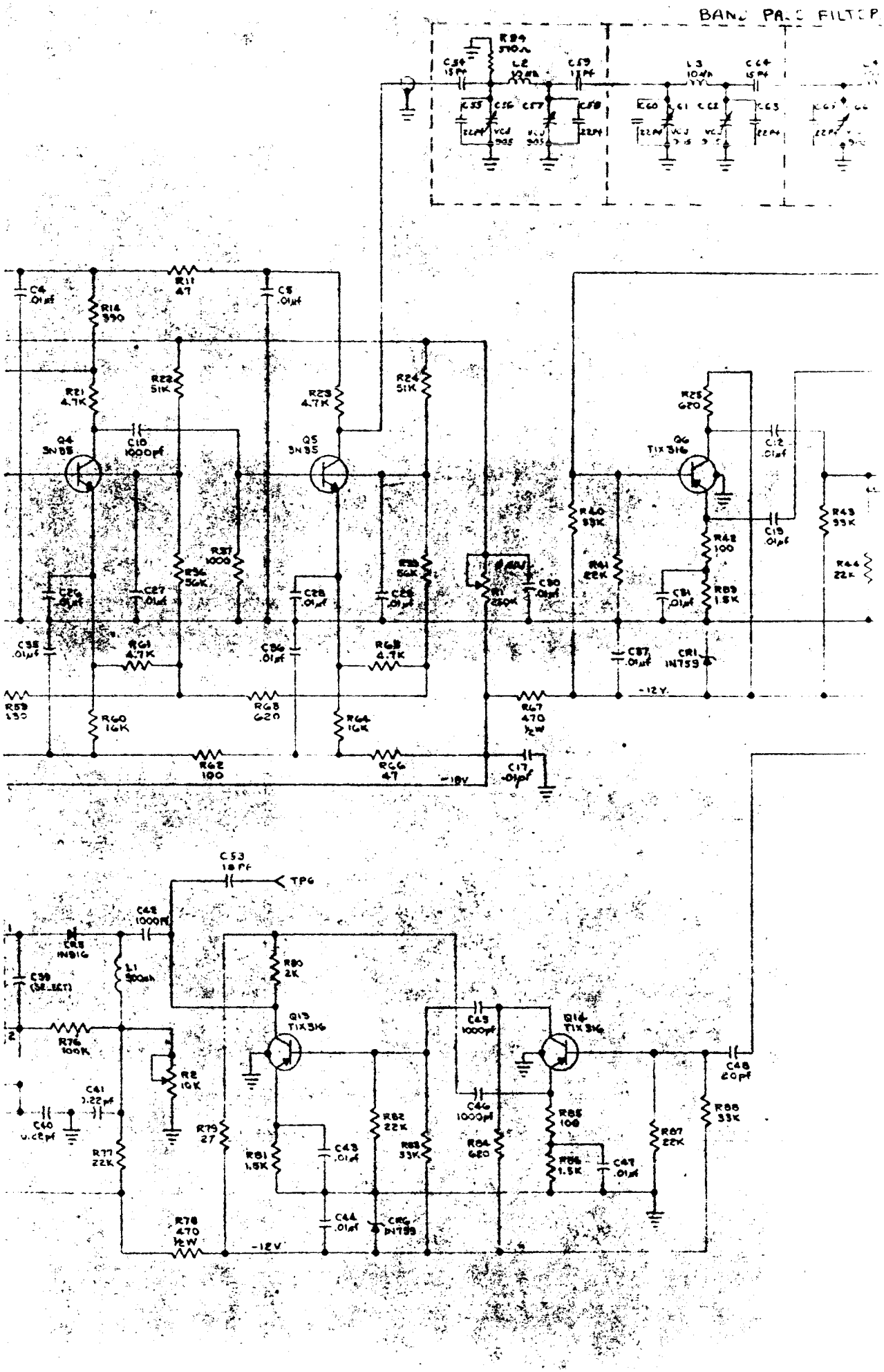
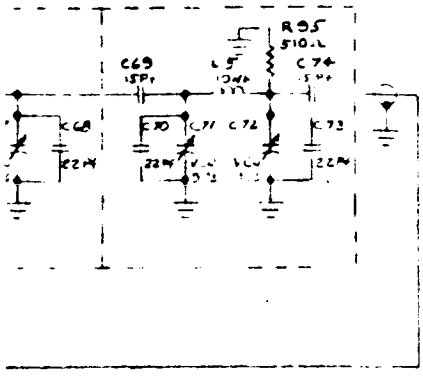
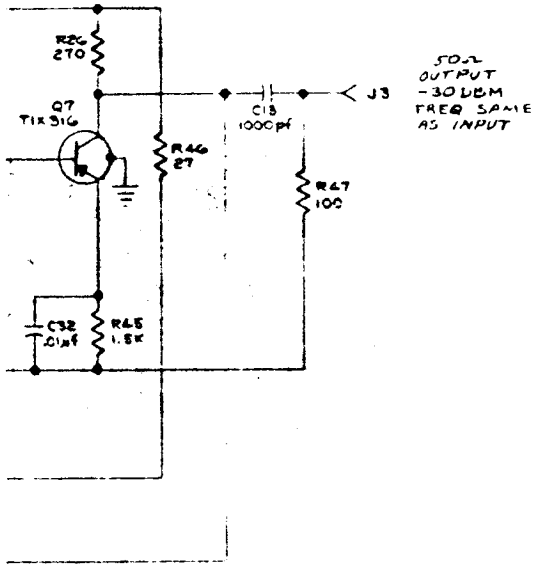


FIG. 8-10 SCHEM., 2ND





NOTES - UNLESS OTHERWISE SPECIFIED:

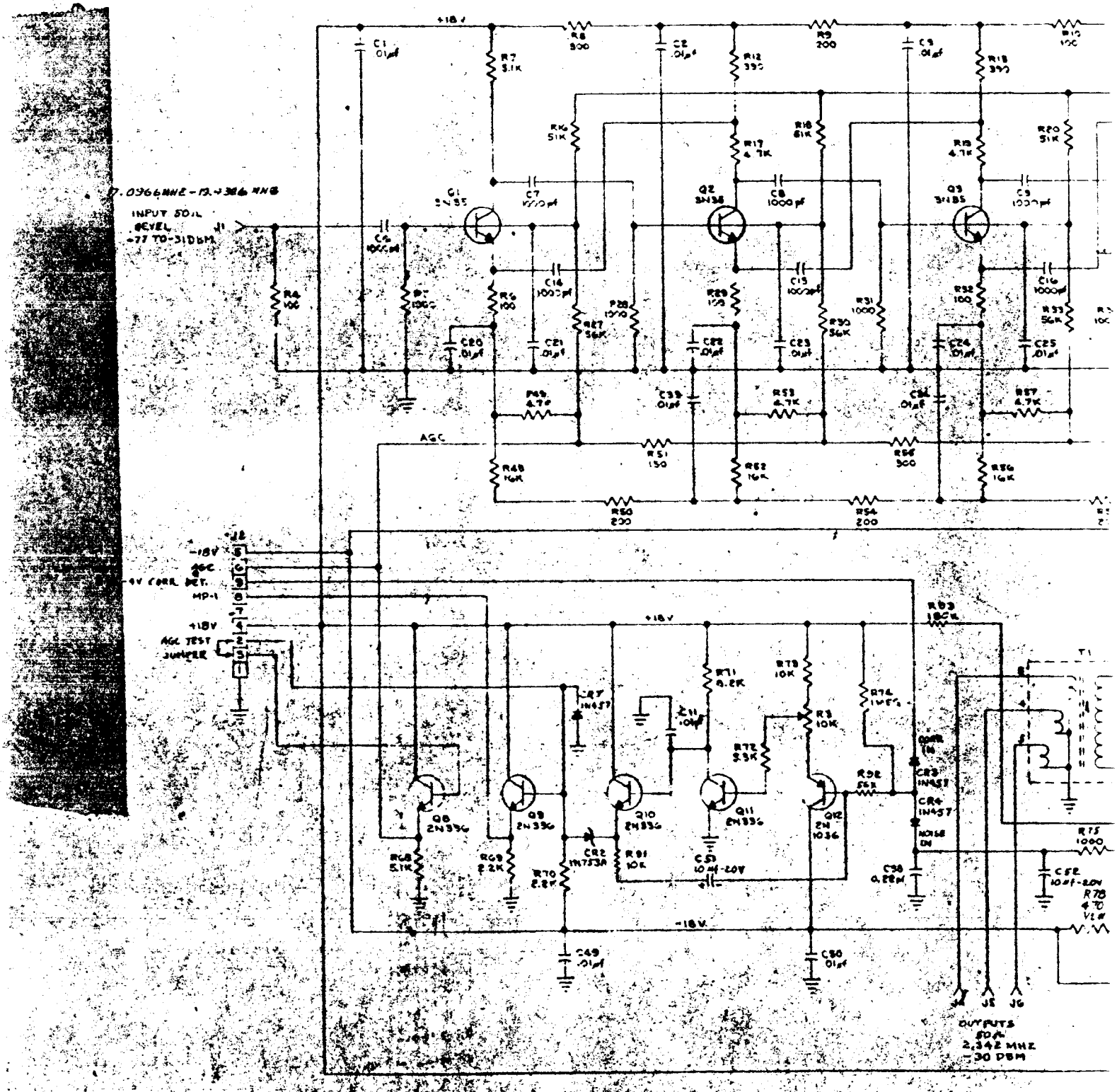
1. ALL RESISTANCE VALUES ARE IN OHMS ± 5%, ½ WATT, INSULATED CARBON.
2. K INDICATES THOUSAND OHMS.
3. R INDICATES TAILORED VALUES

LAST NUMBERS USED
R95 J6 C74 Q14
CR7 L9 T1

NUMBERS NOT USED
R15 C18
R35
R38
R90

REFERENCE DESIGNATIONS ARE ABBREVIATED
PREFIX THE DESIGNATION WITH SCHEMATIC DWG NO

I F AMPLIFIER – AROD CHANNEL NO. 2 A18420


+18 V
INPUT 50Ω
LEVEL
-77 TO -31 DBM
AGC
-18V
AGC
-4V CORR. SET.
MP-1
+18V
AGC TEST
JUMPER
-18 V.
OUTPUTS
50Ω
2.342 MHZ
-30 DBM

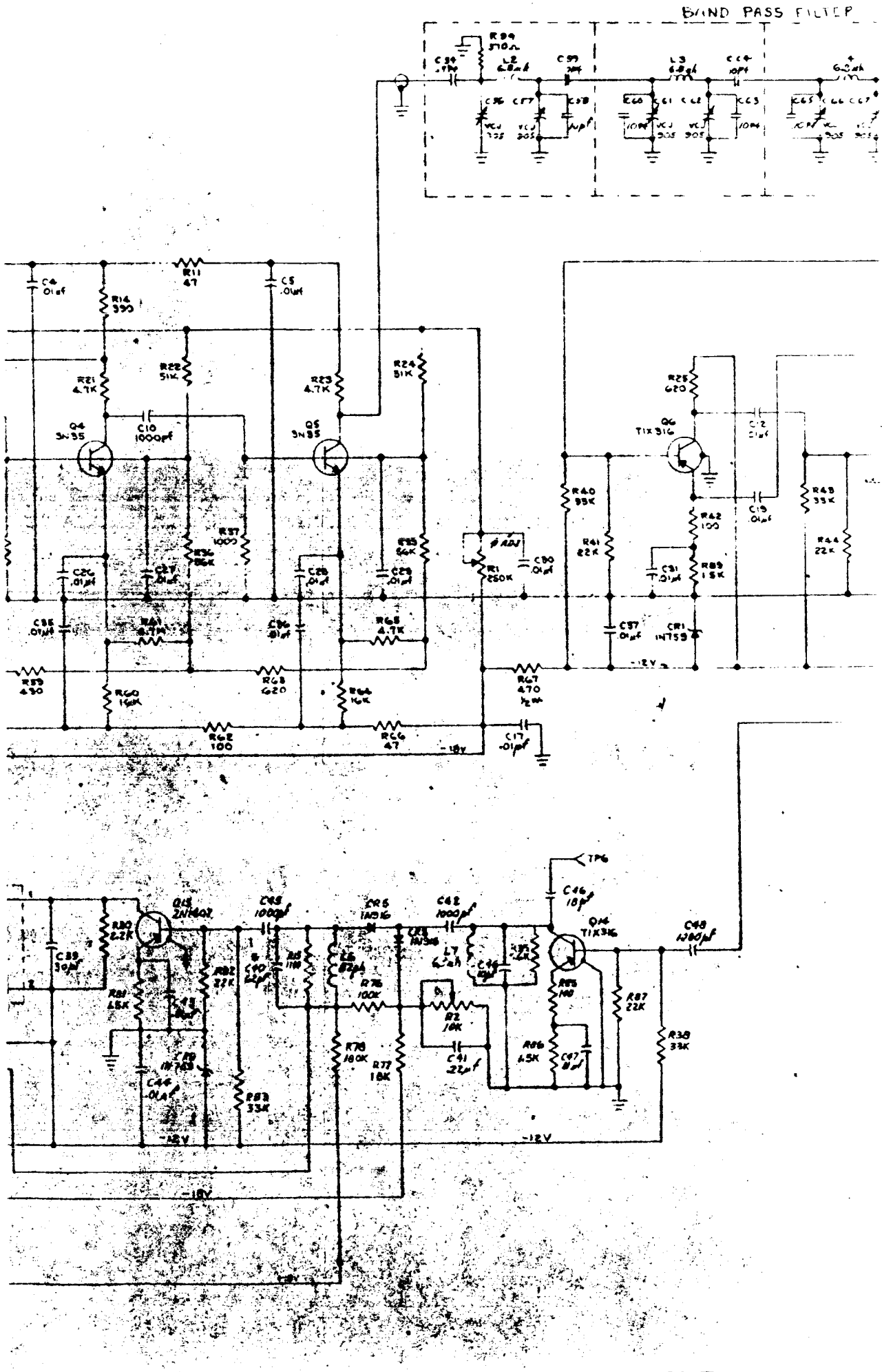
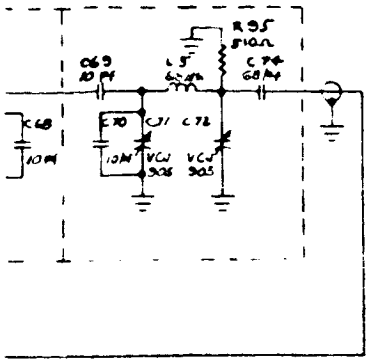
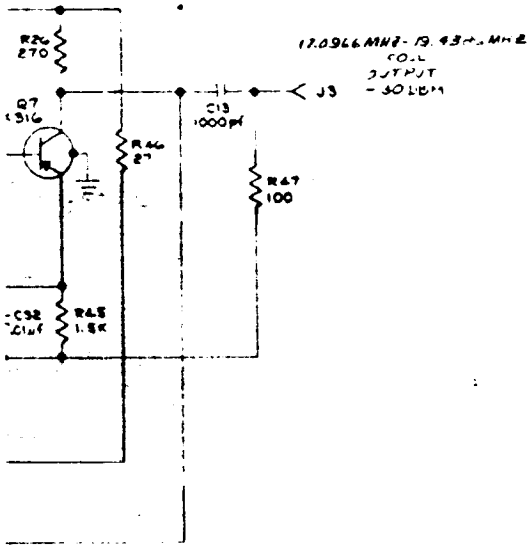


FIG. 8-11 SCHEM., 2ND





17.0966 MHz - 19.43 MHz
COIL
OUTPUT
- 30 DBM

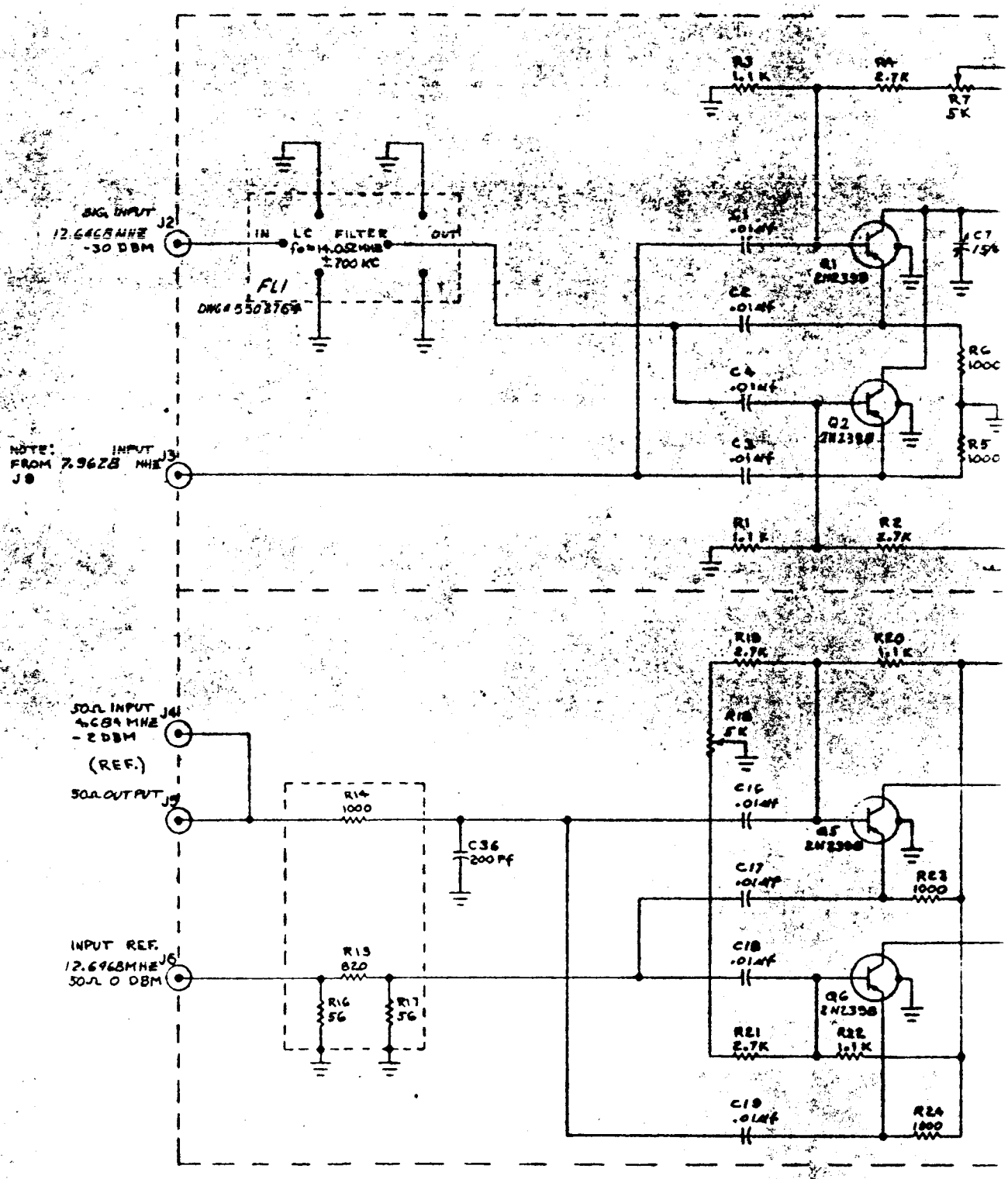
NOTES - UNLESS OTHERWISE SPECIFIED:
1. ALL RESISTANCE VALUES ARE IN OHMS ±5%, ½ WATT, INSULATED CARBON.
2. K INDICATES THOUSAND OHMS.
3. # SELECT C40 VALUE FOR RESONANCE AT 2.342 MHz

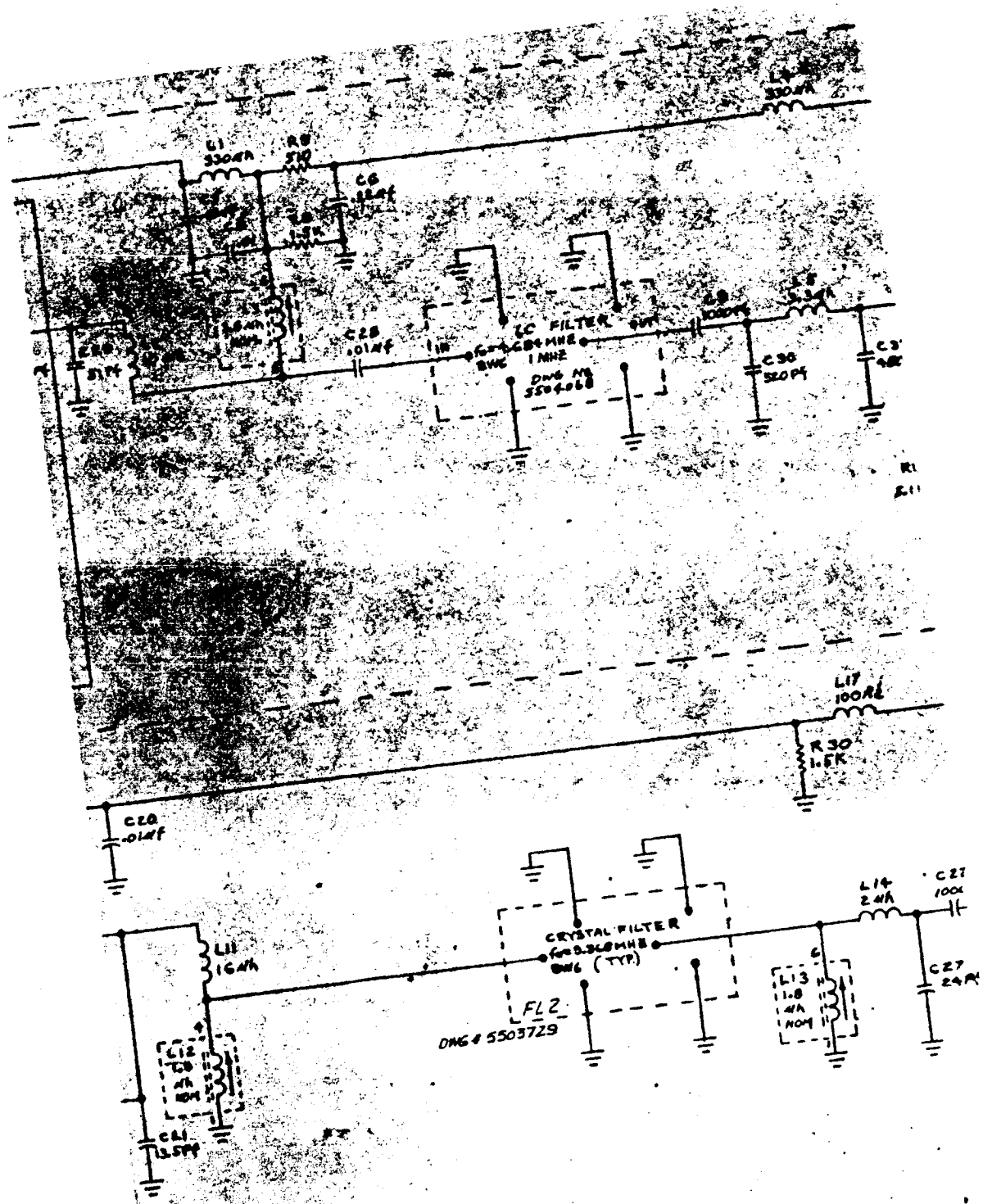
LAST NUMBERS USED
R95 J6 C74 Q14
CR8 L7 S1

NUMBERS NOT USED
C18 L1
C73
C55
R38
R90
R79
R84
R88

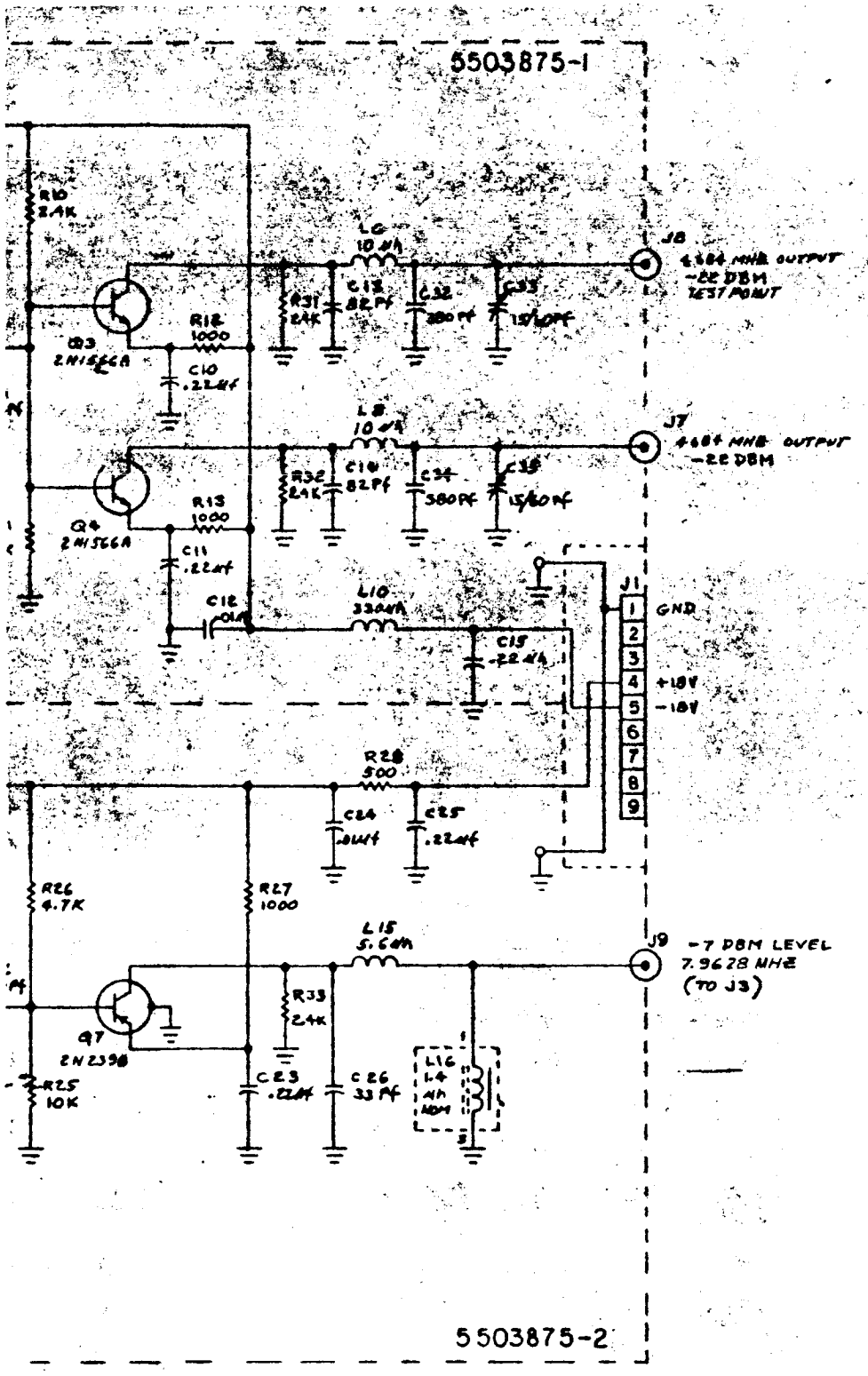
REFERENCE DESIGNATIONS ARE ABBREVIATED
PREFIX THE DESIGNATION WITH SCHEMATIC DWG NO.

IF AMPLIFIER – AROD CHANNEL NO. 3 A18620


SIG. INPUT J2
12.6468MHZ
-30 DBM
IN
LC FILTER
fo=14.052MHZ
±700 KC
OUT
FL1
DWG#5503769
NOTE:
FROM 7.962B MHZ
J8
INPUT J3
R3 1.1K
R4 2.7K
R7 5K
C1 .01MF
Q1 2N2369
C7 15PF
C2 .01MF
C4 .01MF
Q2 2N2369
C3 .01MF
R6 100Ω
R5 100Ω
R1 1.1K
R2 2.7K
50Ω INPUT J4
4.684 MHZ
-2 DBM
(REF.)
50Ω OUTPUT J5
INPUT REF. J6
12.696BMHZ
50Ω 0 DBM
R14 100Ω
C36 200 PF
R15 820
R16 56
R17 56
R10 2.7K
R20 1.1K
R18 5K
C16 .01MF
Q5 2N2369
C17 .01MF
R23 100Ω
C18 .01MF
Q6 2N2369
R21 2.7K
R22 1.1K
C19 .01MF
R24 100Ω


L1 330uH
R9 510
C6
C28 .01uF
LC FILTER
DWG NO 5504068
C30 520 PF
L17 100uH
R30 1.5K
C20 .01uF
CRYSTAL FILTER
DWG (TYP)
FL2
DWG # 5503729
L14 2uH
C27 100
C27 24PF
L11 16uH
L12
C41 3.5PF
L13

3RD IF CONVE



LAST NUMBERS USED			NUMBERS NOT USED	
R33	C36	L18	R29	L7
Q7	J9			L9
				L18

NOTES:

1. REFERENCE DESIGNATIONS ARE ABBREVIATED. PREFIX DESIGNATION WITH SCHEMATIC DWG. NO.

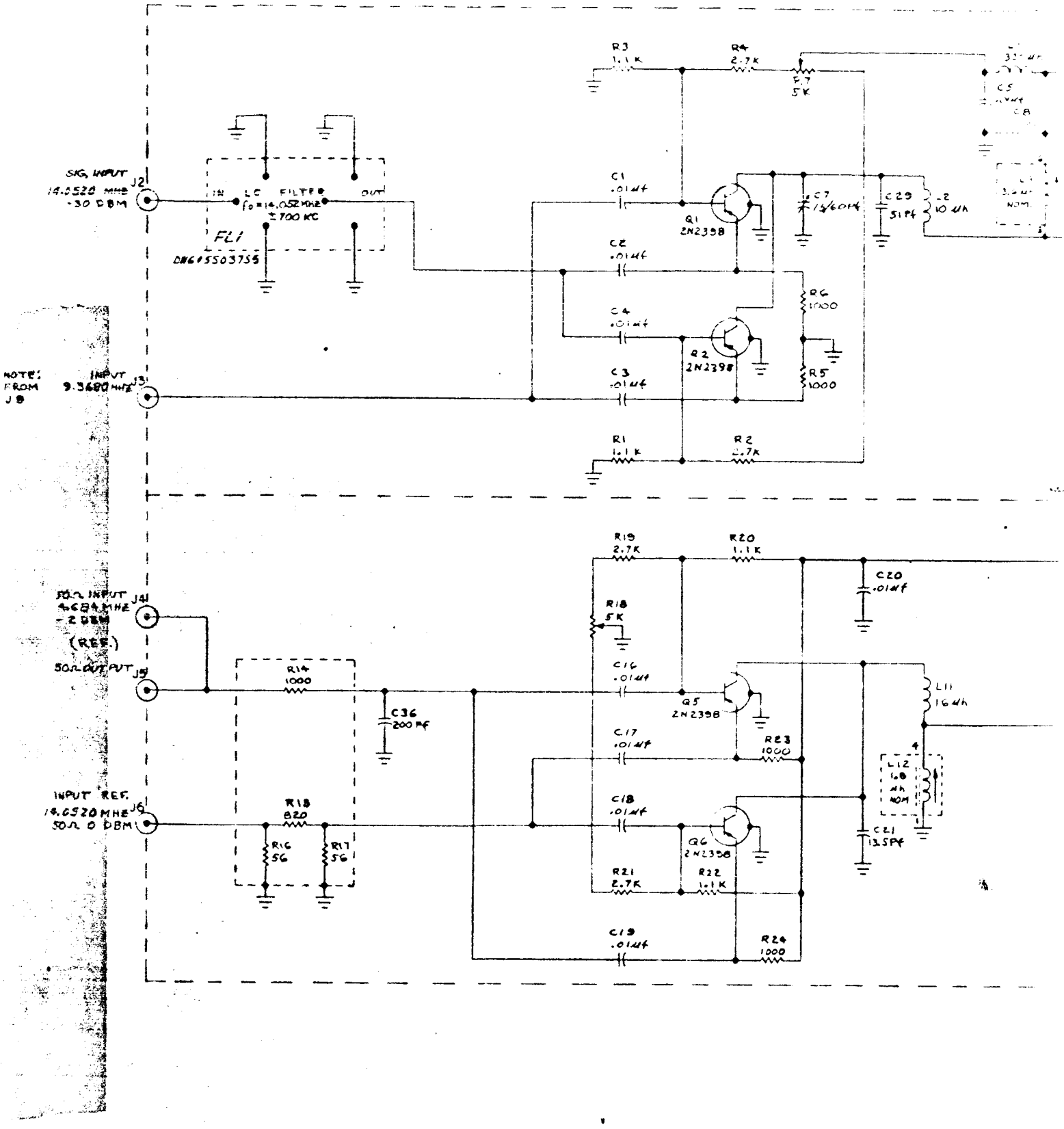
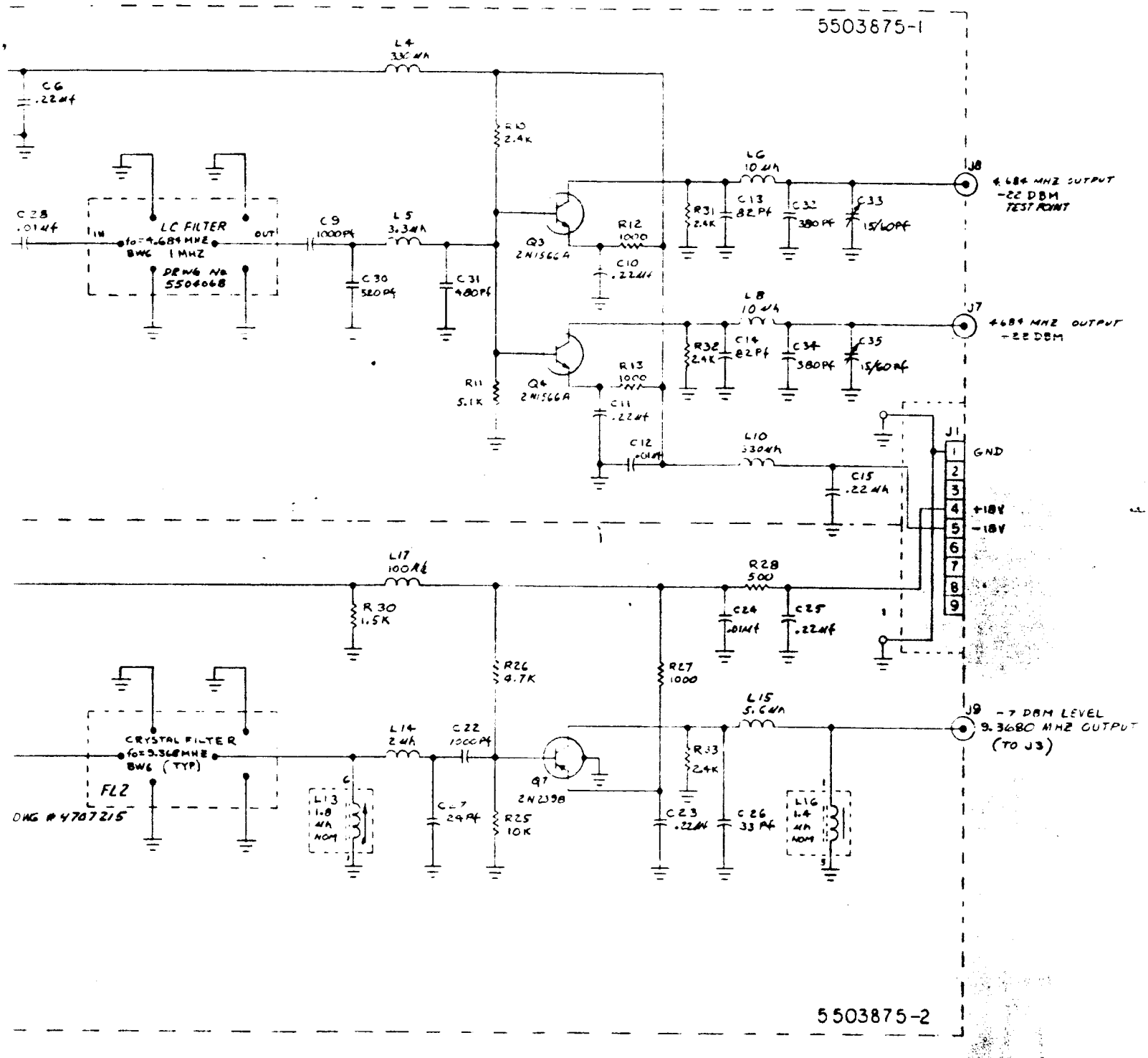

SIG. INPUT
14.0520 MHz
-30 DBM
J2
IN
LC FILTER
f_o = 14.052 MHz
± 700 KC
OUT
FL1
DBG#5503735
R3
1.1K
R4
2.7K
R7
5K
C5
C8
C1
.01 uf
Q1
2N2398
C7
15/60 pf
C29
51 pf
L2
10 uh
C2
.01 uf
C4
.01 uf
C3
.01 uf
R6
100Ω
R5
100Ω
Q2
2N2398
R1
1.1K
R2
2.7K
NOTE:
FROM
J8
INPUT
9.3680 MHz
J3
R19
2.7K
R20
1.1K
C20
.01 uf
R18
5K
50Ω INPUT
4.684 MHz
-2 DBM
(REF.)
J4
50Ω OUTPUT
J5
C16
.01 uf
Q5
2N2398
L11
16 uh
R14
100Ω
C36
200 pf
C17
.01 uf
R23
100Ω
L12
1.8 uh
NOM
INPUT REF.
14.0520 MHz
50Ω 0 DBM
J6
R15
820
C18
.01 uf
R16
56
R17
56
Q6
2N2398
C21
13.5 pf
R21
2.7K
R22
1.1K
C19
.01 uf
R24
100Ω

FIG. 8-13



LAST NUMBERS USED			NUMBERS NOT USED	
R33	C36	L18	R29	L7
Q7	J9			L9
				L18

NOTES:
1 REFERENCE DESIGNATIONS ARE ABBREVIATED. PREFIX DESIGNATION WITH SCHEMATIC DWG. NO.

SCHEM., 3RD I F CONVERTER-AROD CHANNEL NO. 2 A18430

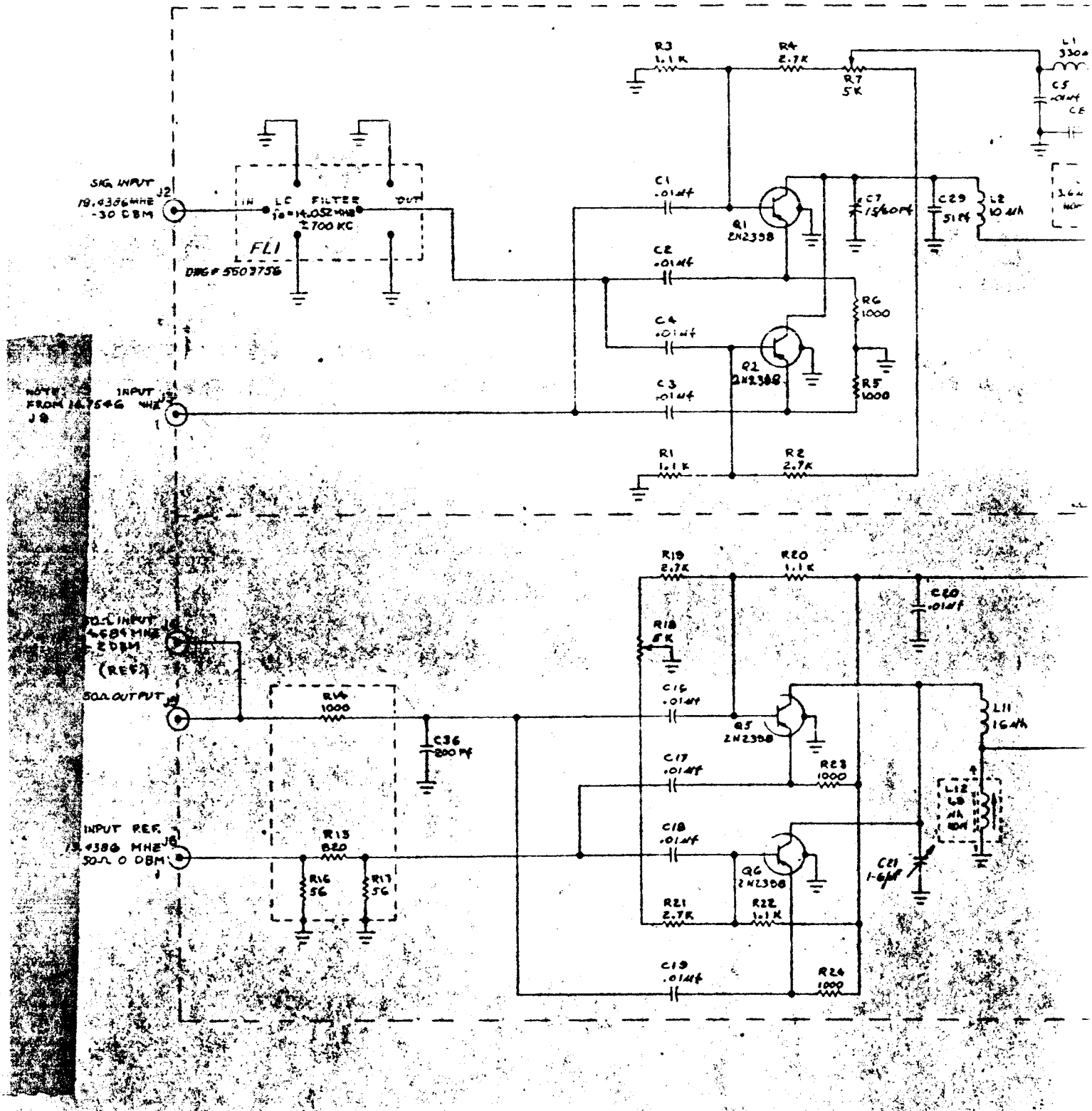
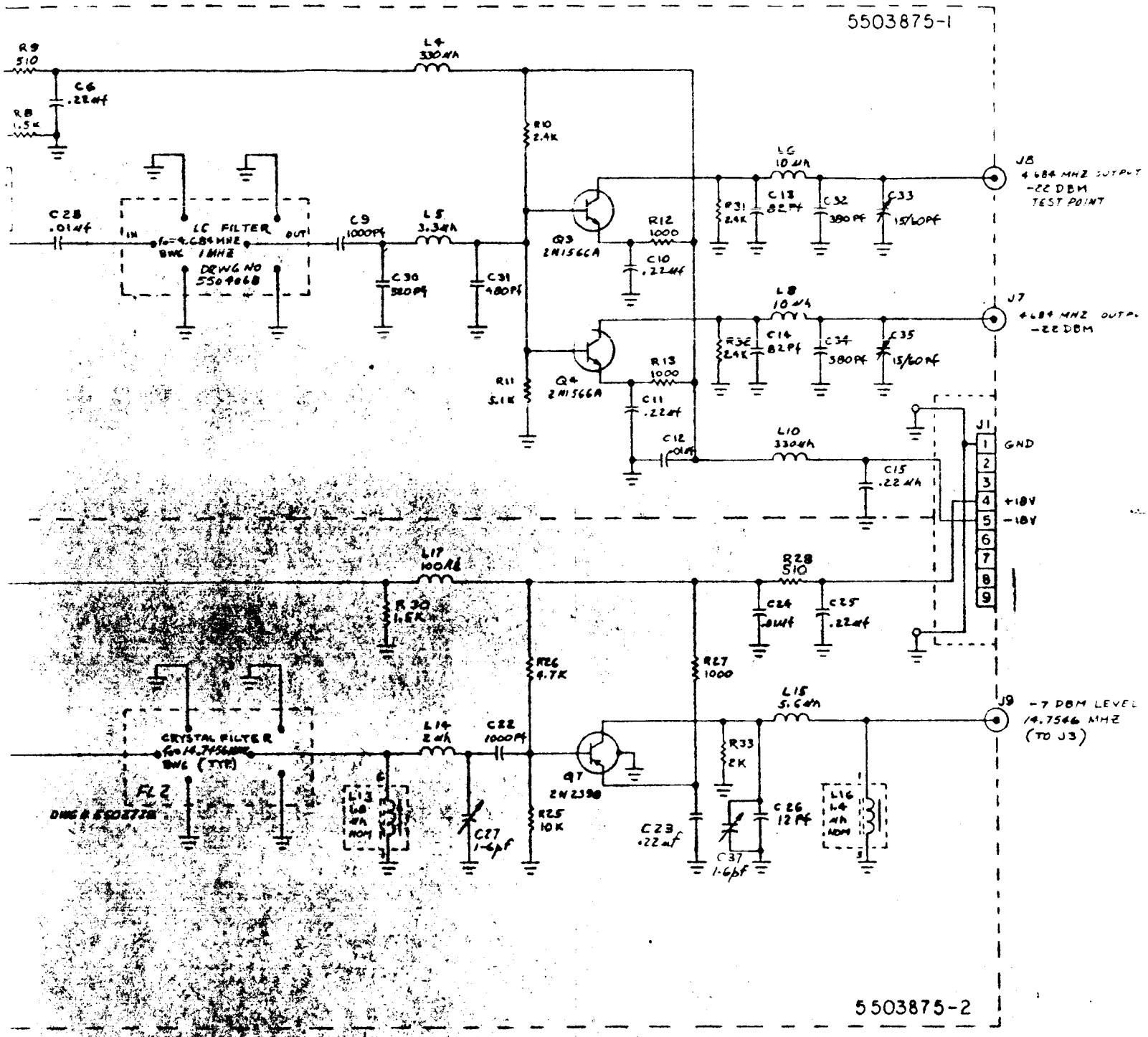

SIG. INPUT
19.4336 MHz
-30 DBM
J2
IN
LC FILTER
OUT
fo = 14.052 MHz
±700 KC
FL1
DWG # 5503756
R3 1.1K
R4 2.7K
R7 5K
C1 .01 µf
C2 .01 µf
C4 .01 µf
C3 .01 µf
Q1 2N2368
C7 15-60 pf
C29 51 pf
L2 10 µh
R6 1000
Q2 2N2368
R5 1000
R1 1.1K
R2 2.7K
NOTE: INPUT FROM 14.7546 MHz J3
J1
R19 2.7K
R20 1.1K
C20 .01 µf
R18 5K
C16 .01 µf
Q5 2N2368
L11 16 µh
C17 .01 µf
R23 1000
C18 .01 µf
Q6 2N2368
C21 1-6 pf
R21 2.7K
R22 1.1K
C19 .01 µf
R24 1000
70 MC INPUT J4
4.684 MHz
2 DBM
(REF)
50Ω OUTPUT J5
R14 1000
C36 200 pf
INPUT REF. J6
14.4386 MHz
50Ω 0 DBM
R13 820
R16 56
R17 56

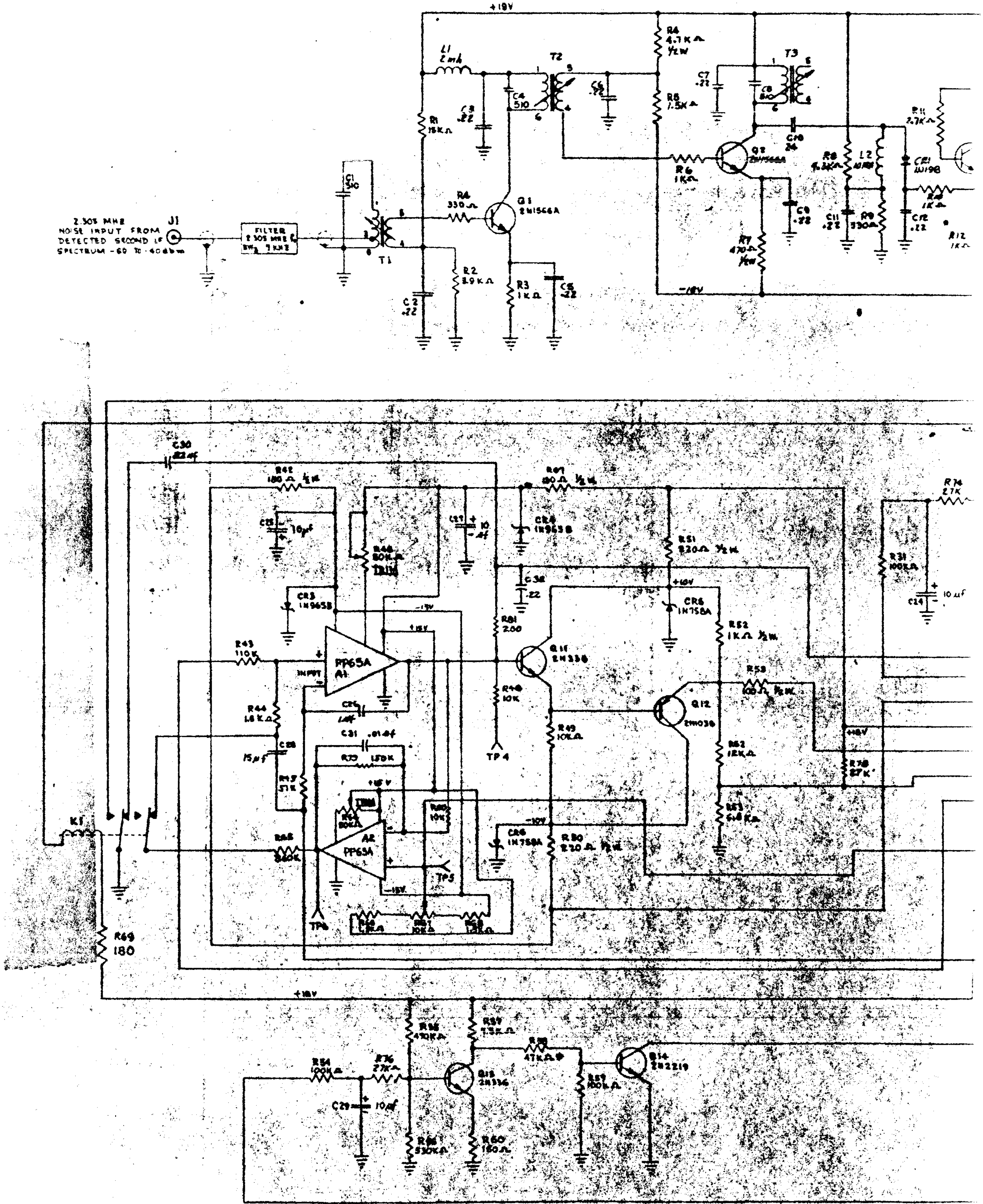
FIG. 8-14

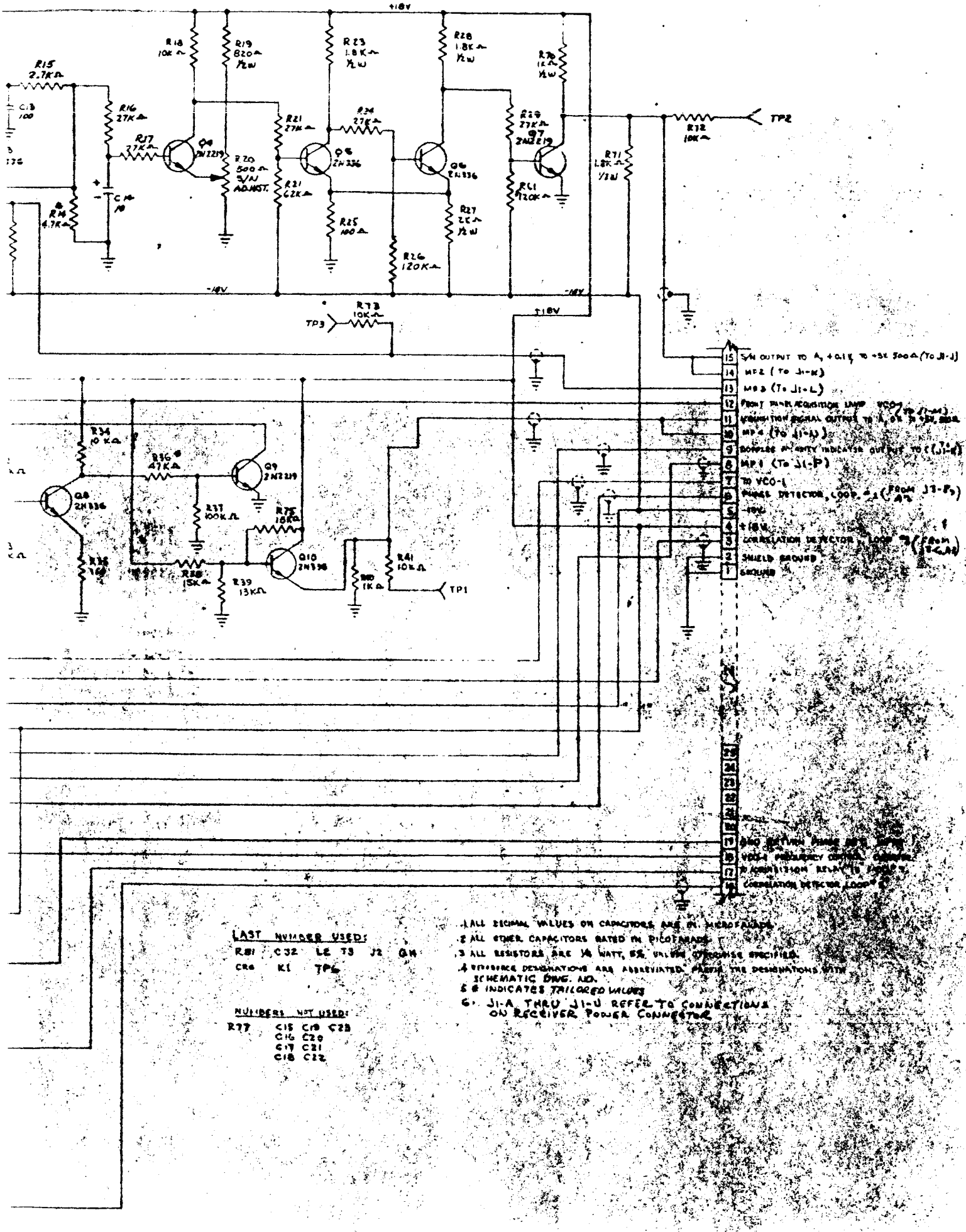


LAST NUMBERS USED			NUMBERS NOT USED		
R33	C37	L18	R29	L7	
Q7	J9			L9	
				L18	

NOTES:
1. REFERENCE DESIGNATIONS ARE ABBREVIATED. PREFIX DESIGNATION WITH SCHEMATIC DWG. NO.

SCHEM., 3RD I F CONVERTER-AROD CHANNEL NO. 3 A18630


+18V
2.305 MHz
NOISE INPUT FROM
DETECTED SECOND I.F.
SPECTRUM -60 TO -40 dbm
J1
FILTER
2.305 MHz
T1
C1
510
R4
330 Ω
Q1
2N1566A
R1
15K Ω
R2
3.9 K Ω
R3
1 K Ω
C5
.22
C2
.22
L1
2 mh
C3
.22
C4
510
T2
C6
.22
R4
4.7 K Ω
½W
R5
1.5 K Ω
C7
.22
T3
R6
1K Ω
Q2
2N1566A
C10
24
R7
470 Ω
½W
C9
.22
C11
.22
R9
330 Ω
C12
.22
L2
R11
2.7K Ω
R12
1K Ω
-18V
C30
R42
180 Ω ½W
C15
10 μf
R46
TRIM
CR3
1N965B
PP65A
A1
INPUT
R43
110K
R44
1.8 K Ω
C28
15 μf
R47
180 Ω ½W
C27
10 μf
CR4
1N965B
C32
.22
R51
820 Ω ½W
+10V
CR5
1N758A
R52
1K Ω ½W
R81
200
R48
10K
TP 4
Q11
2N338
R49
10K Ω
Q12
2N1038
R53
100 Ω ½W
R62
12K Ω
R63
6.8 K Ω
R78
27K
R74
2.7K
R31
100K Ω
C24
10 μf
+18V
C31
.01 μf
R73
150K
TRIM
A2
PP65A
R80
10K
-10V
CR6
1N758A
R50
820 Ω ½W
TP5
TP6
K1
R69
180
+18V
R55
470K Ω
R57
1.5K Ω
R58
47K Ω
R54
100K Ω
R76
27K Ω
Q13
2N336
Q14
2N2219
R59
100K Ω
C29
10 μf
R56
330K Ω
R60
150 Ω



LAST NUMBER USED:

R81 C32 LE T3 J2 QH

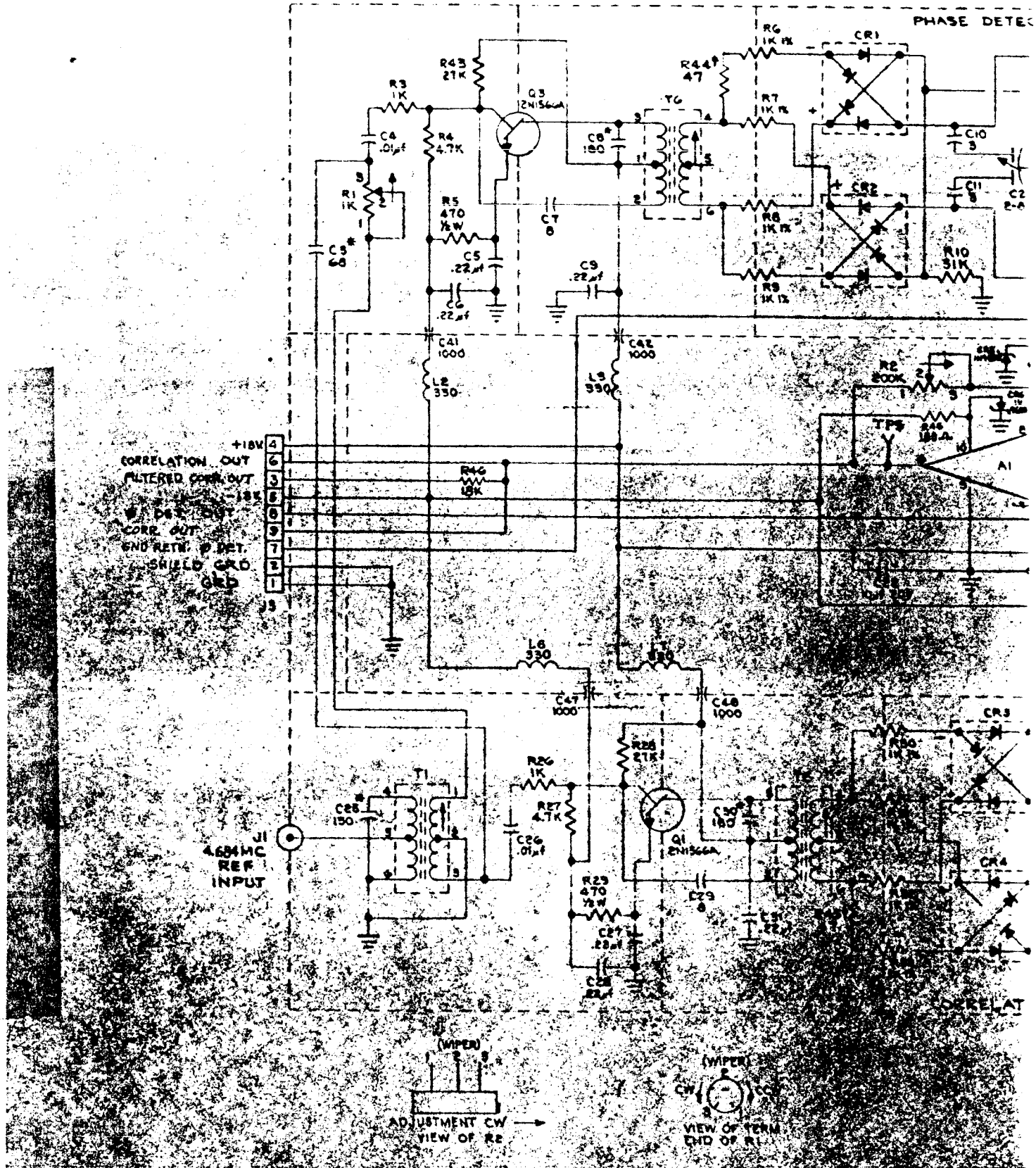
CR6 K1 TP6

NUMBERS NOT USED:

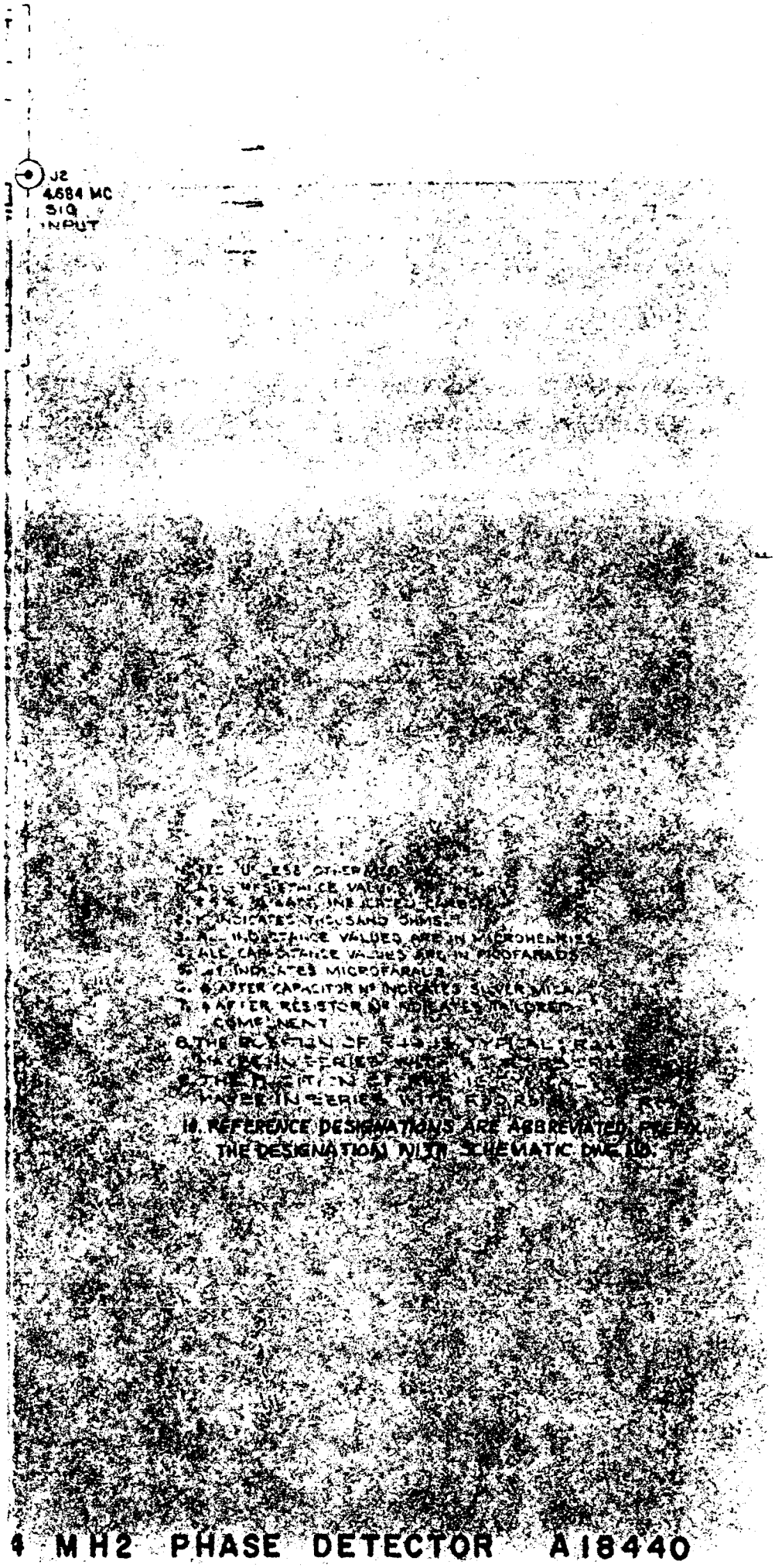
R77 C15 C19 C28
C16 C20
C17 C21
C18 C22

1. ALL DECIMAL VALUES ON CAPACITORS ARE IN MICROFARADS.
2. ALL OTHER CAPACITORS RATED IN PICOFARADS.
3. ALL RESISTORS ARE ¼ WATT, 5% UNLESS OTHERWISE SPECIFIED.
4. REFERENCE DESIGNATIONS ARE ABBREVIATED. PREFIX THE DESIGNATIONS WITH SCHEMATIC DWG. NO.
5. # INDICATES TAILORED VALUES
6. J1-A THRU J1-U REFER TO CONNECTIONS ON RECEIVER POWER CONNECTOR

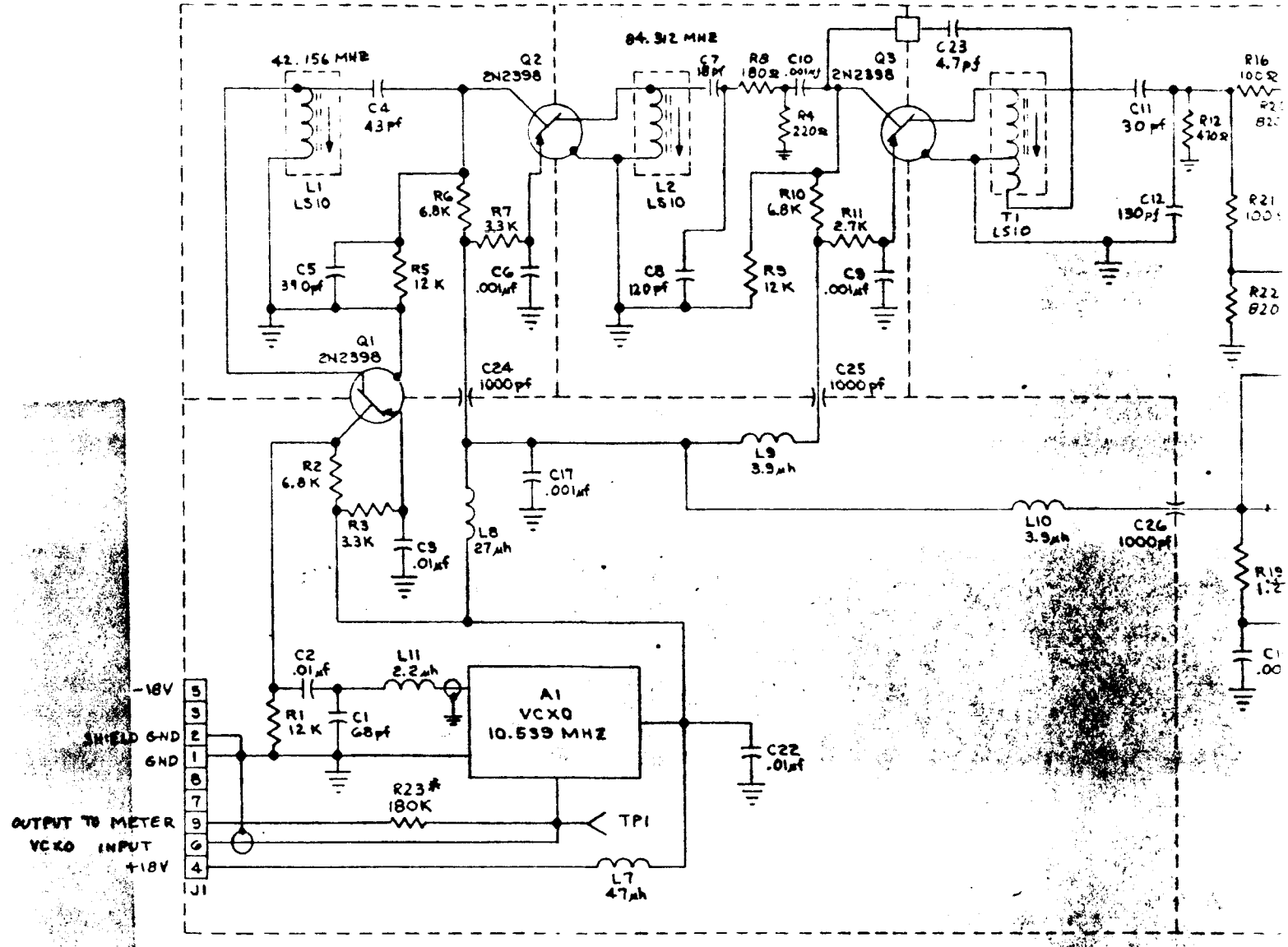
FIG. 8-16 SCHEM., PHASE LOCK LOOP FILTER A18450



TG	LS10	RED	CW	SOL	58	3	25	1	—	—	5	2	52	4	16	5	14	6			870700B-4
T5	LS10	RED	CW	SOL	30	5	7	1	—	—	2	2	39	4	20	5	20	6			870700B-5
T4	LS10	RED	CW	SOL	32	4	28	3	—	—	3	6	32	2	11	—	6	11			870700B-2
T3	LS10	RED	CW	SOL	30	5	7	1	—	—	2	2	30	4	20	5	20	6			870700B-5
T2	LS10	RED	CW	SOL	32	3	25	1	—	—	5	2	32	4	14	5	14	6			870700B-4
T1	LS10	RED	CW	SOL	32	4	28	3	—	—	3	6	32	1	8	2	8	5			870700B-1
SYMBOL NO.	PCBM NO.	COLOR OF WIRE	DIR	TYPE OF WIND	PRIMARY SIZE OF WIRE	PRIMARY START TERM NO.	PRIMARY TURNS TO TAP	PRIMARY TERM	PRIMARY TURNS TO FINAL	PRIMARY FINAL TERM	SECONDARY SIZE OF WIRE	SECONDARY START TERM NO.	SECONDARY TURNS TO TAP	SECONDARY TERM	SECONDARY TURNS TO FINAL	SECONDARY FINAL TERM	CT	TERM NO.	COIL DWG. NO.		

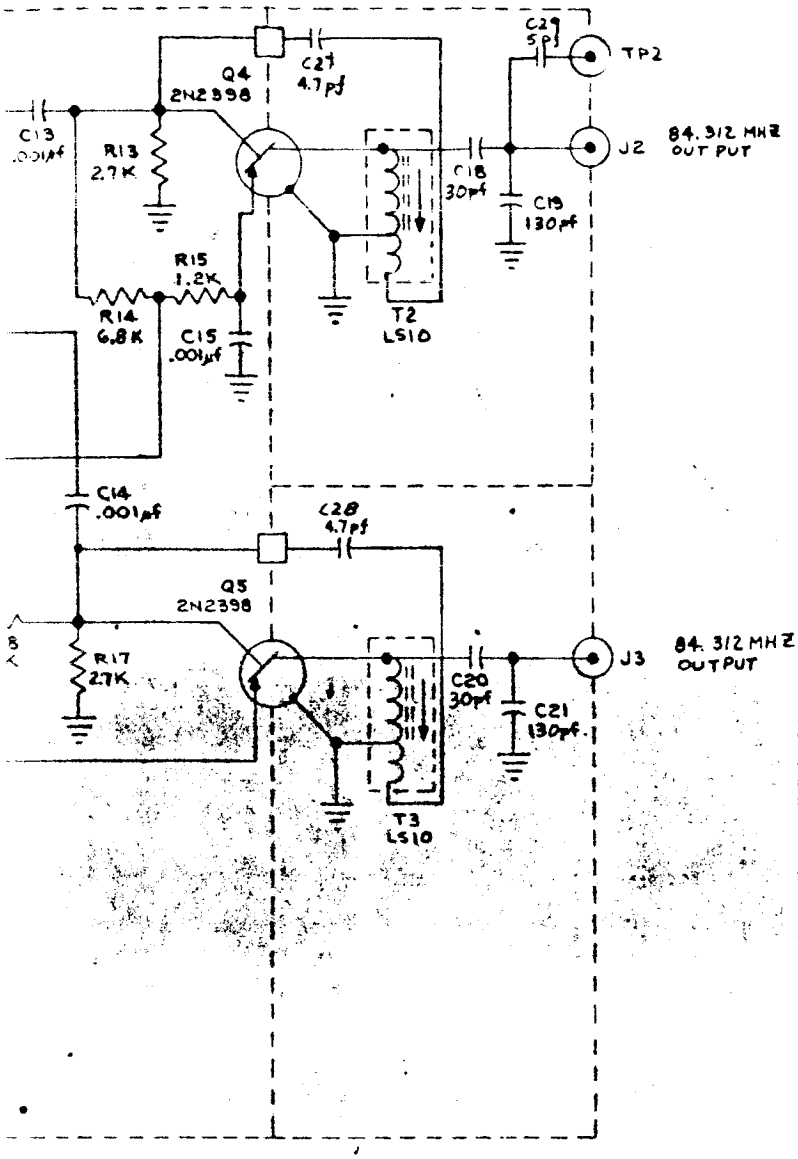


4 MH2 PHASE DETECTOR A18440



LAST NUME
R23 C29
A1 J3 TE

SYMBOL NO.	FORM NO.	COLOR OF SLUG	DIR.	TYPE OF WINDING	PRIMARY: SIZE OF WIRE	START TERM NO.	TURNS TO TAP #1	TERM.	TURNS TO TAP #2	TERM.	TURNS TO FINAL	FINAL TERM.	SECONDARY: SIZE OF WIRE	START TERM NO.	TURNS TO TAP #1	TERM.	TURNS TO FINAL	FINAL TERM.	IND. NOM.	TERM NO.	
T3	LS10	WHT			22	1	3.5	4			2.0	2									
T2	LS10	WHT			22	6	3.5	4			2.0	5									
T1	LS10	WHT			22	1	3.5	2			2.0	6									
L2	LS10	WHT			22	1					4.5	4									
L1	LS10	GRN			26	1					13	4									



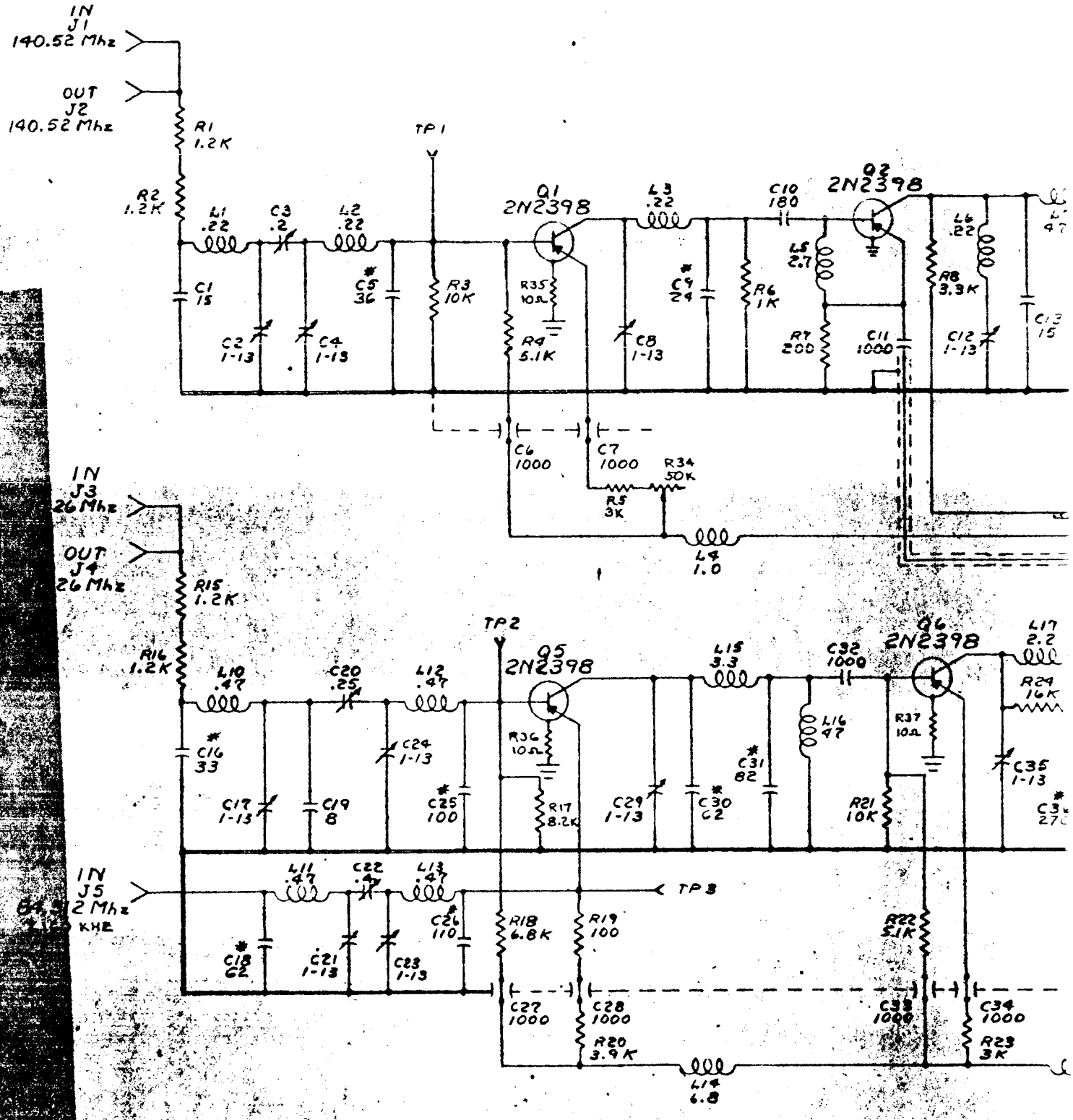
NOTES - UNLESS OTHERWISE SPECIFIED:
1. ALL RESISTANCE VALUES ARE IN OHMS ±5%, ½ WATT, INSULATED CARBON.
2. K INDICATES THOUSAND OHMS.
3. # INDICATES TAILORED VALUE

REFERENCE DESIGNATIONS ARE ABBREVIATED. PREFIX TH
DESIGNATION WITH SCHEMATIC DWG. NO.

S USED
11 Q5

NUMBERS NOT USED
L3, L4, L5, L6

FIG. 8-17 SCHEM., V C O - 1 A18460



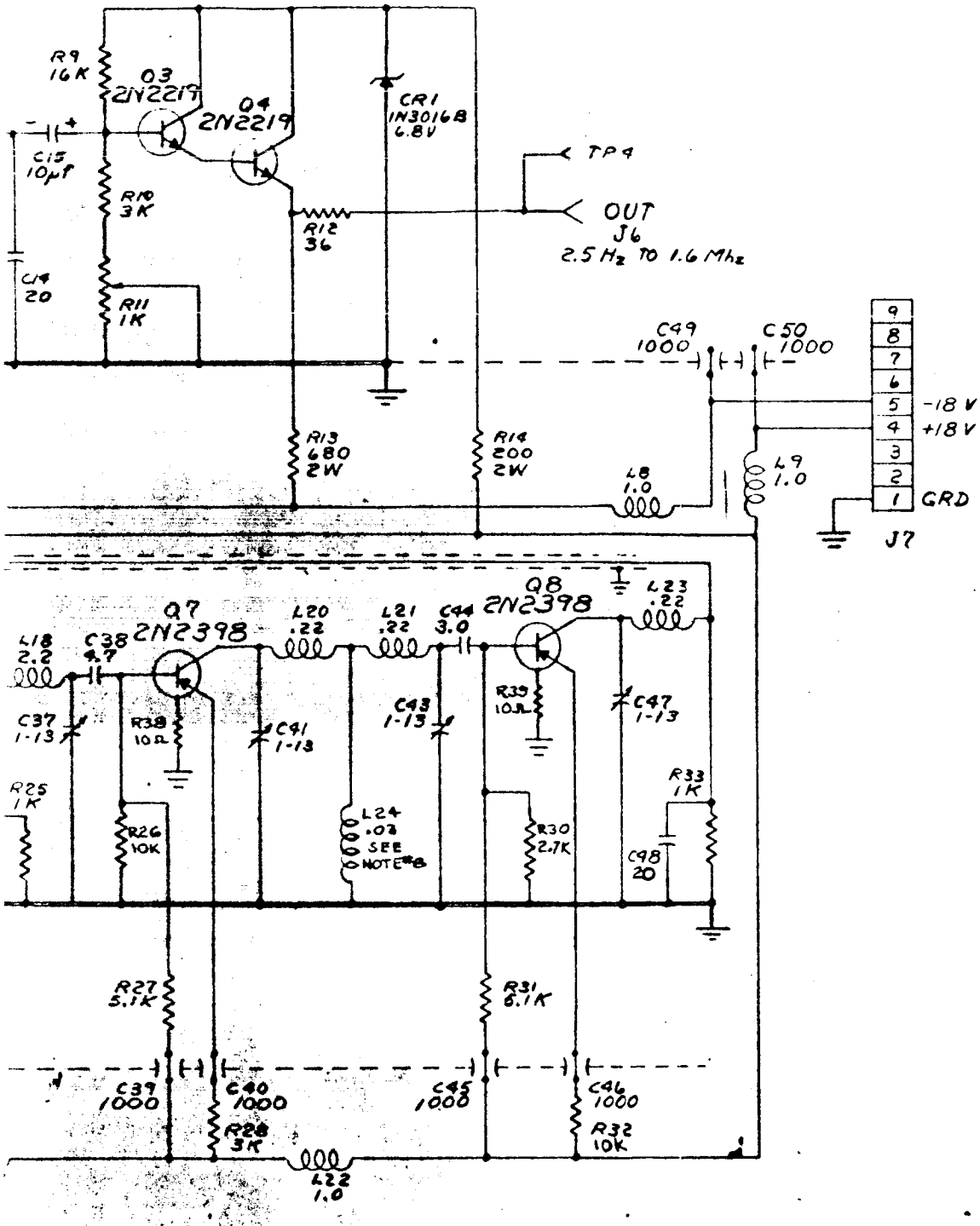
NOTE: UNLESS OTHER WISE SPECIFIED

1. ALL RESISTANCE VALUES ARE IN OHMS ±5%, ¼W
2. K INDICATES THOUSAND OHMS.
3. ALL CAPACITANCE VALUES ARE IN PICOFARADS.
4. ALL INDUCTANCE VALUES ARE IN MICROHENRIES.
5. μF INDICATES MICROFARADS.
6. * AFTER CAPACITOR NUMBER DESIGNATES SILVER MICA.
7. C3, C20 & C22 ARE FABRICATED COMPONENTS MADE OF SILVER PLATED COPPER RIBBON
8. L24 = 3T *20 BUS, .111 I.D. (34 DRILL) TURNS SPACED ABOUT 2X WIRE DIAMETER.
9. REFERENCE DESIGNATIONS ARE ABBREVIATED, PREFIX THE DESIGNATION WITH SCHEMATIC DWG. NO.

LAST N
J7 CR1
TP4 Q8

NUMBERS
R29 C

FIG



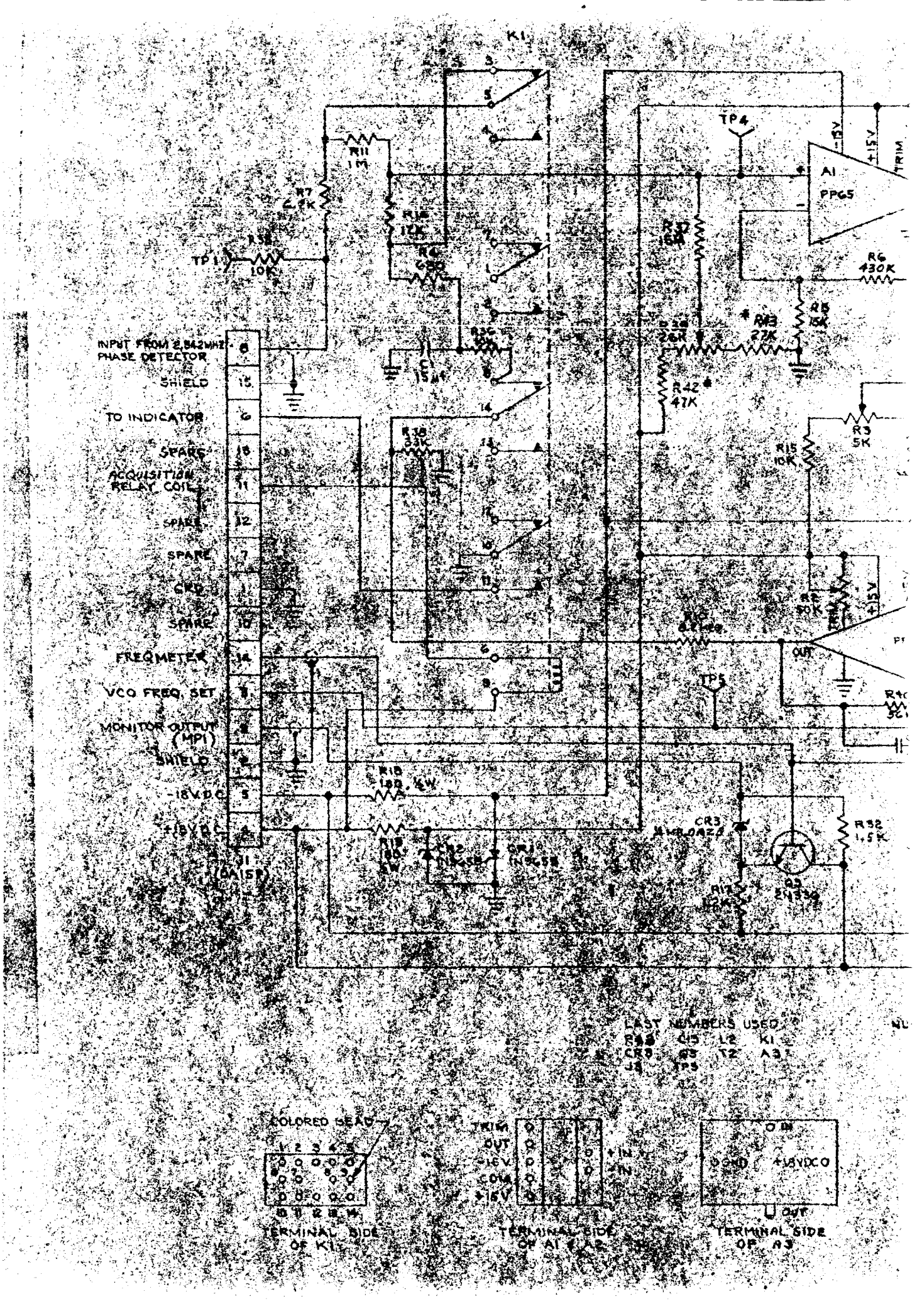
BER USED :

70 L24

39

USED

8-18 SCHEM., DOPPLER DETECTOR A18500


K1
TP4
-15V
+15V
TRIM
A1
PPG5
R11 1M
R7 2K
R18 12K
R6 680
TP1
R38 10K
R37 16R
R6 430K
R5 15K
R43 27K
R36 100K
C1 15μF
R42 47K
INPUT FROM 2.842MHz PHASE DETECTOR
SHIELD
TO INDICATOR
SPARE
ACQUISITION RELAY COIL
SPARE
SPARE
CR2
SPARE
FREQMETER
VCO FREQ. SET
MONITOR OUTPUT (MP1)
SHIELD
-18V DC
+18V DC
J1 (DA15P)
R38 33K
R3 5K
R15 10K
R2 50K
R40 8.2K
OUT
TP5
R10 180Ω ½W
R19 180Ω ½W
CR2 IN4458
CR1 IN4458
CR3 MMBZ5231B
R32 1.5K
Q3 2N3904
R17 2K
LAST NUMBERS USED:
R38 C15 L2 K1
CR3 Q3 T2 A3
J1 TP5
COLORED BEAD
TERMINAL SIDE OF K1
TRIM
OUT
-15V
COM
+15V
+IN
-IN
TERMINAL SIDE OF A1 & A2
O IN
GND
+18VDC
OUT
TERMINAL SIDE OF A3

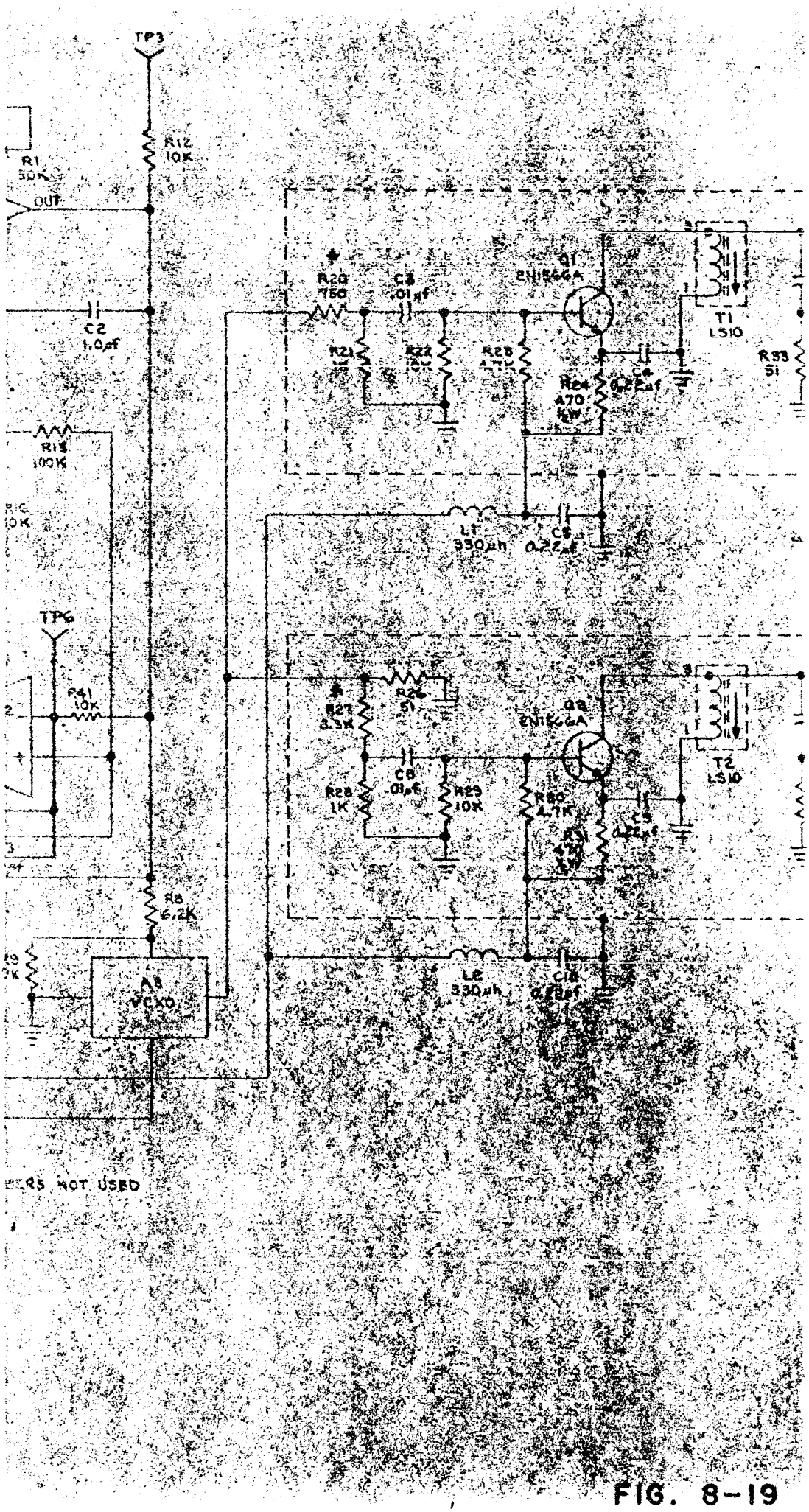
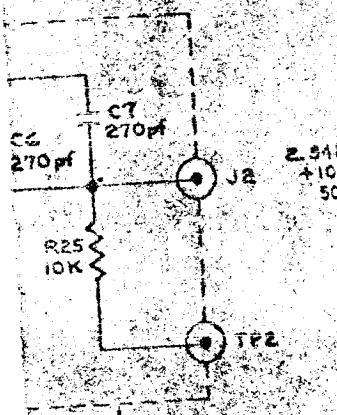
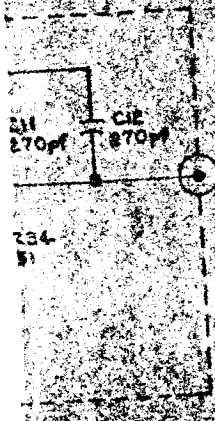
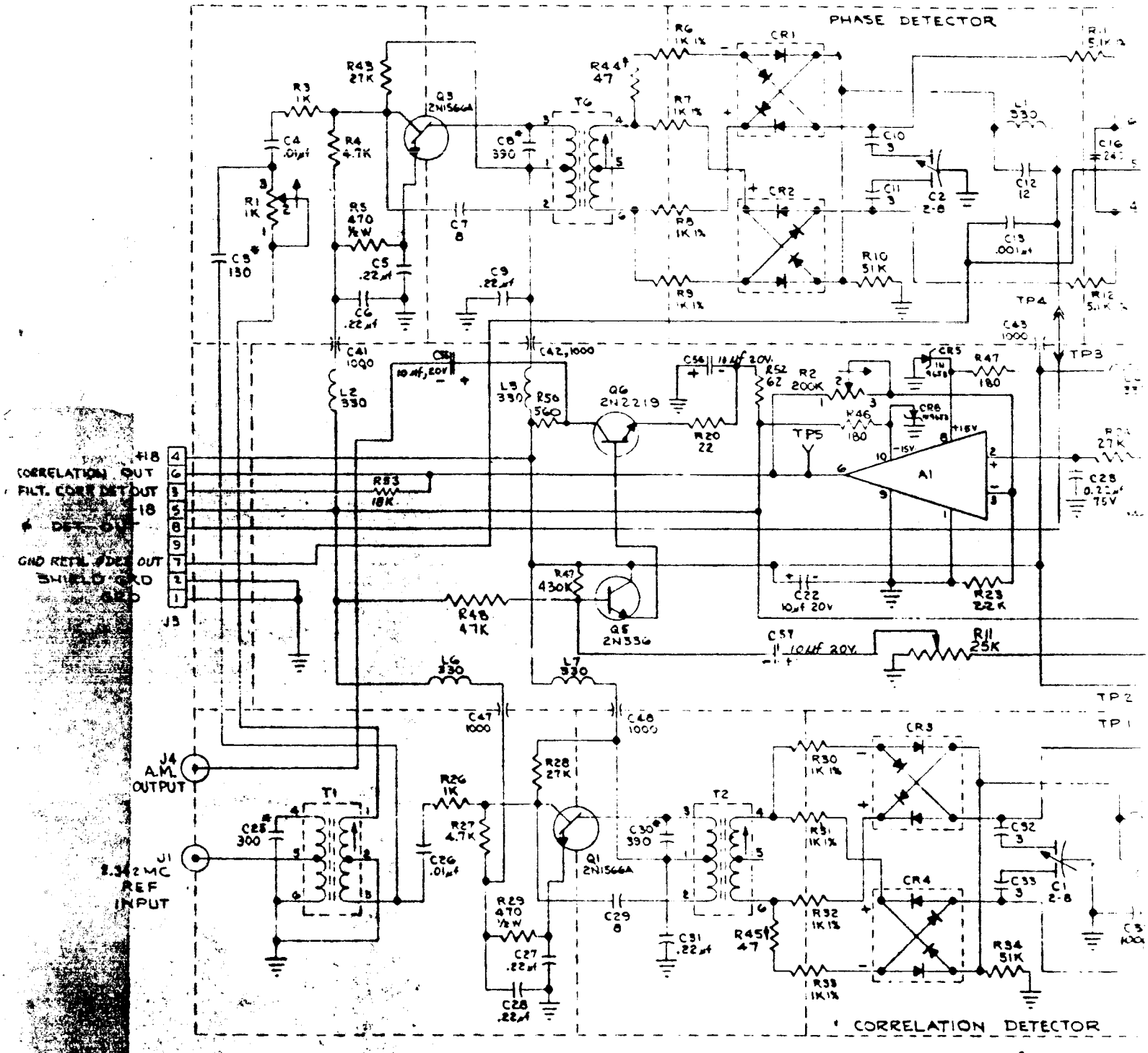

TP3
R12
10K
R1
50K
OUT
C2
1.0μF
R13
100K
TP6
R41
10K
R8
6.2K
A8
VCXO
R20
750
C8
.01μF
Q1
2N5644A
T1
LS10
R21
R22
10K
R23
4.7K
R24
470
C9
0.22μF
R33
5i
LT
330μH
C9
0.22μF
R26
51
R27
2.3K
Q2
ENI6CGA
T2
LS10
C6
.01μF
R28
1K
R29
10K
R30
4.7K
R31
470
C9
0.22μF
Le
330μH
C18
0.22μF

FIG. 8-19



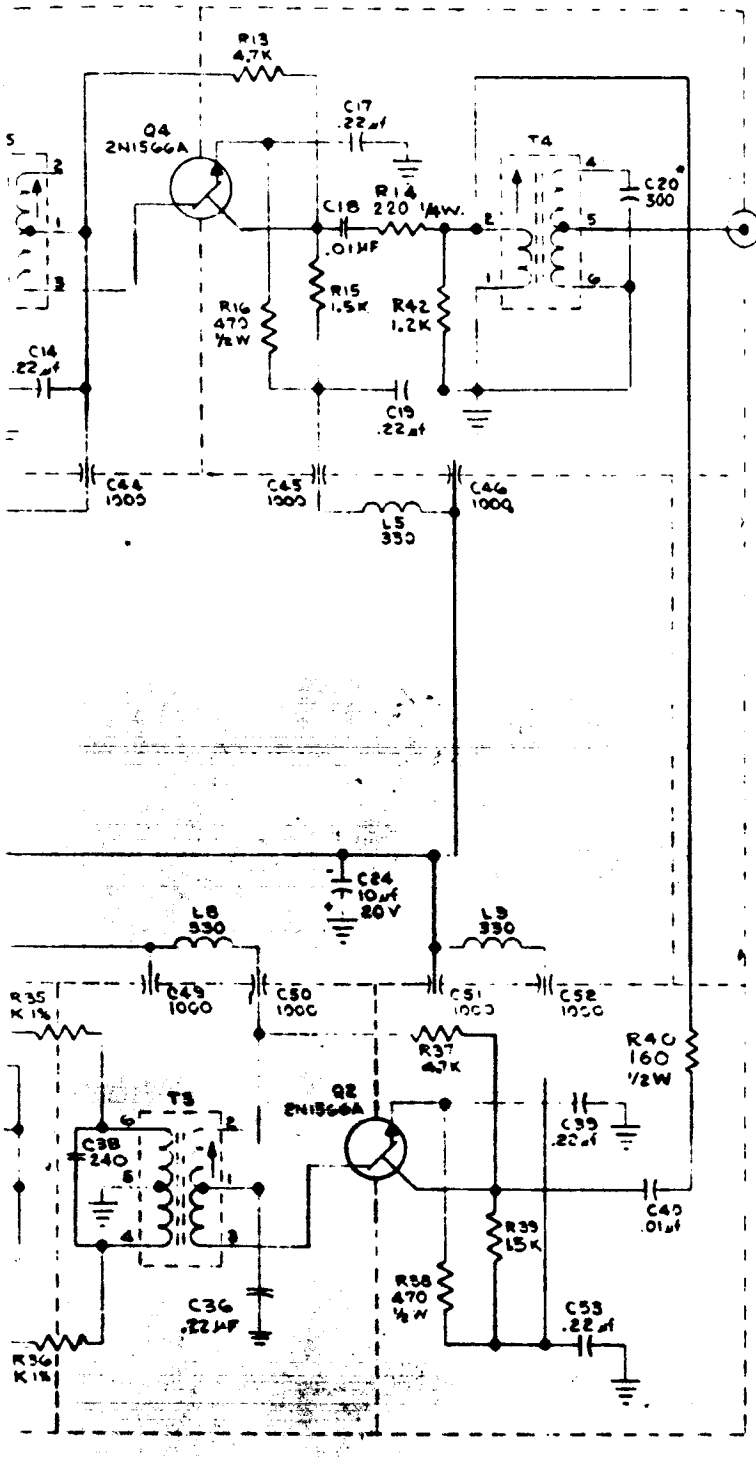


NOTES - UNLESS OTHERWISE SPECIFIED:
1. ALL RESISTANCE VALUES ARE IN OHMS ±5%, ¼ WATT, INSULATED CARBON.
2. K INDICATES THOUSAND OHMS.
3. # INDICATES TAILORED VALUES.
4. REFERENCE DESIGNATIONS ARE ABBREVIATED; PREFIX THE DESIGNATION WITH SCHEMATIC DWG. NO.



SYMBOL NO.	FORM NO.	COLOR OF SWG	D.R.	PRIMARY TYPE OF WINDING	PRIMARY SIZE OF WIRE	PRIMARY START TERM NO.	PRIMARY TURNS TO TAP	PRIMARY TERM.	PRIMARY TURNS TO TAP 2	PRIMARY TERM.	PRIMARY TURNS TO FINAL	PRIMARY FINAL TERM.	SECONDARY SIZE OF WIRE	SECONDARY START TERM NO.	SECONDARY TURNS TO TAP	SECONDARY TERM.	SECONDARY TURNS TO FINAL	SECONDARY FINAL TERM.	NO. INCH LBS	TERM NO.	COIL DWG
T6	LS10	RED	CW	SOL	32	3	37	1	—	—	7	2	32	4	21	5	21	6		1-3	4707008-7
T5	LS10	RED	CW	SOL	32	3	10	1	—	—	3	2	32	4	30	5	30	6		4-6	4707008-8
T4	LS10	RED	CW	SOL	32	4	38	5	—	—	4	6	32	2	—	—	9	1		4-6	4707008-9
T3	LS10	RED	CW	SOL	32	3	10	1	—	—	3	2	32	4	30	5	30	6		4-6	4707008-8
T2	LS10	RED	CW	SOL	32	3	37	1	—	—	7	2	32	4	21	5	21	6		1-3	4707008-7
T1	LS10	RED	CW	SOL	32	4	38	5	—	—	4	6	32	1	7	2	7	3		4-6	4707008-6

FIG



NOTES - UNLESS OTHERWISE SPECIFIED:

1. ALL RESISTANCE VALUES ARE IN OHMS ± 5%, 1/8 WATT, INSULATED CARBON.
2. K INDICATES THOUSAND OHMS.
3. ALL INDUCTANCE VALUES ARE IN MICROHENRIES
4. ALL CAPACITANCE VALUES ARE IN PICOFARADS.
5. µf INDICATES MICROFARADS.
6. * AFTER CAPACITOR Nº INDICATES SILVER MICA OR DURA-MICA
7. ♦ AFTER RESISTOR Nº INDICATES TAILORED COMPONENT
8. THE POSITION OF R44 IS TYPICAL; R44 MAYBE IN SERIES WITH R6, R7, R8, OR R9.
9. THE POSITION OF R45 IS TYPICAL; R45 MAYBE IN SERIES WITH R30, R31, R32, OR R33
10. REFERENCE DESIGNATIONS ARE ABBREVIATED. PREFIX THE DESIGNATION WITH SCHEMATIC DWG. NO

LAST NUMBERS USED

C58, J4, L10, CR8
Q6, R53, T6,
A2, TP5, CR6,

NUMBERS NOT USED

C15, C37, R17, R18, R19,
C21, R26, R32, R40, R39,
C57

3-20 SCHEM., 2.342 M H 2 PHASE DETECTER A18470

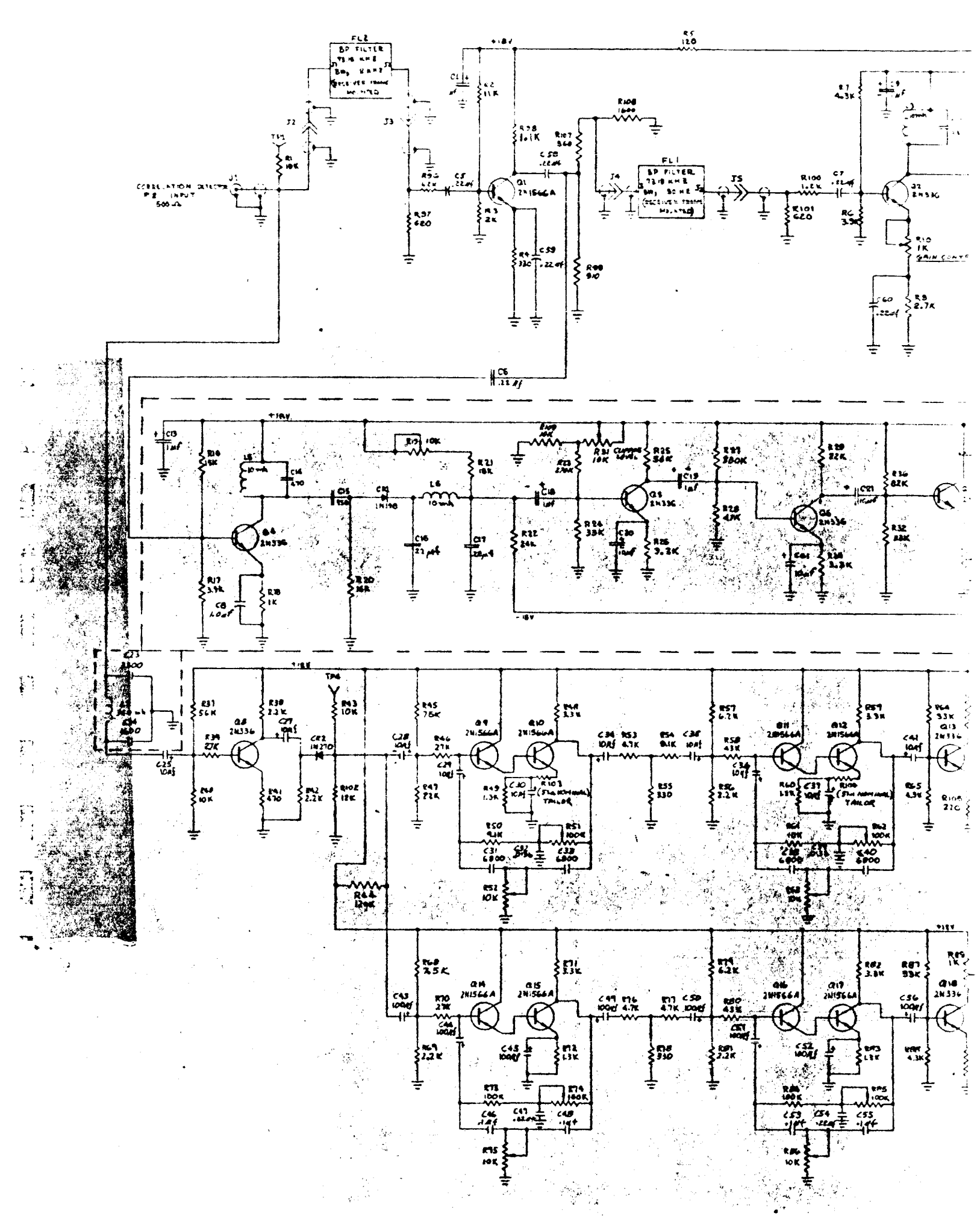
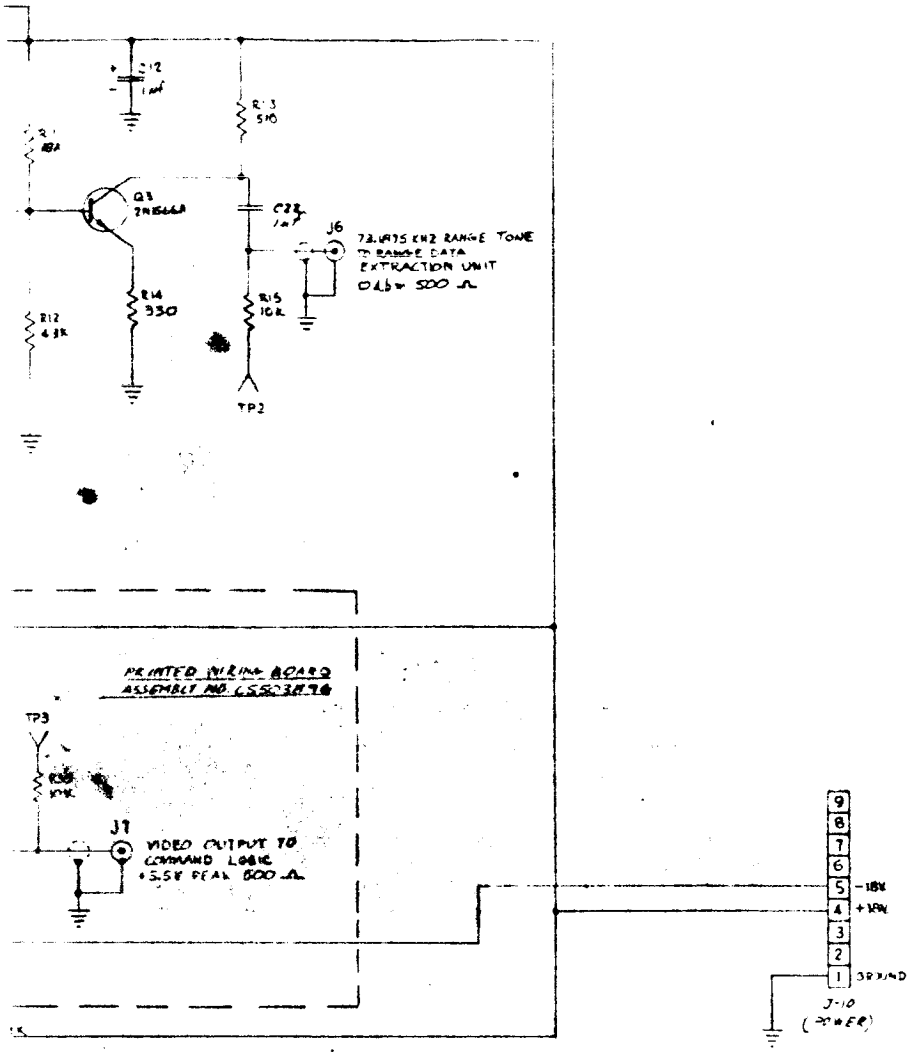
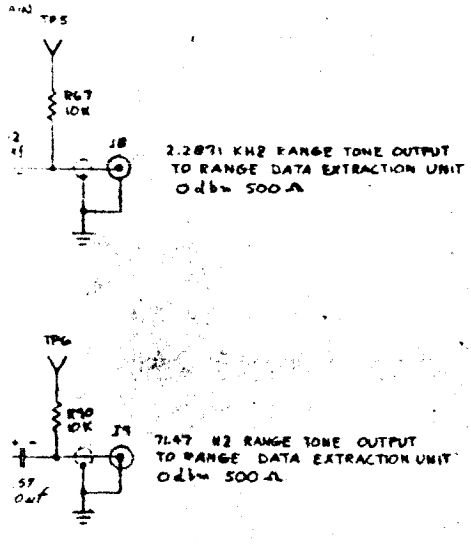


FIG. 8-21





NOTES: UNLESS OTHERWISE SPECIFIED;
1. ALL RESISTANCE VALUES ARE IN OHMS (K=1000 M=1000000), 1/8 W, 5%
2. ALL CAPACITANCE VALUES ARE IN μf
3. REFERENCE DESIGNATIONS ARE ABBREVIATED. PREFIX DESIGNATIONS WITH SCHEMATIC DWG. NO.

LAST NO. USED;
C41, CR2, L7, Q18, R109

NUMBERS NOT USED;
L1 C2 R8
L2 C3 R33
L4 C4
C26

HEM., RANGE TONE EXTRACTION A18490

A P P E N D I X A

Test data of Receiver Channels No. 1 and 3 is presented here. This data was taken without benefit of a frequency synthesizer or input signal simulator. Therefore, it may not reflect the performance of the receiver when operating with the actual signals to be received.

15151 Bledsoe Street

San Fernando, California

telephone EMpire 7-2211

Federal LABORATORIES

Chicago
Fort Wayne
Palo Alto
San Fernando
Nutley

AROD FINAL TEST DATA

Channel # 1

REQUIRED REFERENCES (Inputs)

To J-12	Frequency	4.684 MHz
	Level	-2.5 dbm
To J-11	Frequency	12.6968 MHz
	Level	-8 dbm
To J-6	Frequency	70.26 MHz
	Level	
To J-9	Frequency	140.52 MHz
	Level	

SPECTRUM SIDETONE LEVELS

High Frequency Carrier	0	db
Low Frequency Carrier	-6	db
73 MHz Sideband	Lower 70% / Upper 30%	db *
1.179 KHz Sideband	-8	db *
1.107 KHz Sideband	-8	db *

* Measured at J-4 on Module No. 2, with respect to the 2.342 MHz signal.

RANGE TONE OUTPUTS

At J-17 Frequency 2.342 MHz

Level 2.3 V P-P 50-Ω Load

At J-13 Frequency 73.1875 KHz

Level 4.0 V P-P, R10 set for 2V P-P

At J-15. Frequency 2.2871 KHz

Level 6V Max, R66 set for 2V P-P (avg.)

At J-16 Frequency 71.47 Hz

Level 2V Max, R89 set for 2V P-P

2 - 1KHz At J4 of A8 Level 5V P-P, R41 Set & locked at -100dbm input signal (96.9588MHz)

73KHz At J4 of A8 Level 0.25 V. P-P

DOPPLER SIGNAL OUTPUT

At J-7 Frequency 2.5 Hz to 1.6 MHz

Level _____ ± _____

DOPPLER POLARITY OUTPUT

At J-1 - R

Volts	Freq. A J-~~2~~ 3 on A-5	4.684 MHz Loop Freq. Meter
+9		
0	84,323,8	+4,5
-9		
-3,85	84.452 MHz	+136
+0,68	84.312 MHz	-6
+8,45	84.172 MHz	-147

VIDEO OUTPUT (3.7.2) * (~~50%~~ 100% Square Wave Modulation of 73 KHz) 30% & 10% SB

Amplitude of 1 KHz Video @ J-14 6 V P-P, R34 set for 2V P-P

Noisy at -100 dbm Input to Module 11

ACQUISITION SIGNAL (3.7.3) * J1-M Somewhat noisy at -90dbm

Level Acquired	-143 dbm	+5,1V at J1-M
Level Unacquired	-144	0 V.

MONITOR POINTS (3.8) *

a. AGC Voltage at J-1 - G

vs Signal into Module 11

Input	Volts at J-1-~~6~~ G	AGC Meter
-143 dbm	2,0	2,6
-142	2,3	2,8
-140	3,9	3,4
-135	3,4	3,9
-130	3,6	4,1
-125	3,75	4,25

* Refers to AROD-SPEC-9, Dated 26 August 1963

VS Signal into Module 11 (Cont.)

Input	Volts at J-1-~~F~~G	AGC Meter
-120 dbm	3.8	4.33
-115	3.9	4.4
-110	3.91	4.42
-105	3.95	4.45
-100	4.0	4.5
- 95	4.30	4.80

b. Acquisition Signal at J-1-~~M~~N

Not Acquired 0 (< 0.001 V)

Acquired + 5.1 V.dc

c. Noise Analog Signal at J-1-L

Input		
	-140 dbm	5.0 V.dc
	-135	4.7
	-130	4.34
	-125	3.96
	-120	3.42
	-115	2.99
	-110	1.33
	-105	0.66
	-100	0.30
	-90	0.12
	-80	0.115

d. Signal-to-Noise Ratio J1-K

Adjust R-13-A4 to switch at designated input levels.

Input Level	On Level	Off Level
-140 dbm	-140 dbm	-139 dbm
~~-110~~ -100	-100	-98
-125	-125	-124

(Leave set at -125 dbm)

Output Voltages

	J1-J	J1-K
ON	5.1	5.1
OFF	0.15	0.15

e. VCO 2 Voltage at J-1-H

J-1-H Volts	Frequency	TP3A7 Volts	2.342 MHz Loop Freq. Meter
3.7	2.342	+1.02	-200
2.58	2.313,205	0	0
1.16	2.3425	-1.51	+280
6.25	2.3415	+3.55	-550 -- off scale!

INPUT POWER

+18 VDC 610 ma

-18 VDC 540 ma

SENSITIVITY

Lowest level to Module 11 where phase-lock Loop #1 stays locked -143 dbm

Lowest level to Module 11 where Loop #2 stays locked

-131 dbm

Lowest level to Module 1 where Loop #1 stays locked

-105 dbm

Lowest level to Module 1 where Loop #2 stays locked

-86 dbm

CORRELATION METERS

RF Level To Module 11	4.684 MHz Loop Corr. Meter	2.342 MHz Loop Corr. Meter
- 90 dbm	4,05	3,68
-100	4,00	4,10
-110	4,0	4,00
-120	4,0	2,41
-130	3,98	0,50
-135	3,95	
-140	3,93	
-142	3,8	
-143	3,25	
-144	2,8	

No Modulation on 2.342 MHz ↓ Signal

-125 dbm = 1.20

NOTE: Relationship of main carrier to modulated carrier (2.342 MHz below main carrier) at input to Module 11 is

+6 db.

PHASE-LOCK LOOP BANDWIDTHS

	3 db BW	Calculated Noise BW
Loop #1	45	
Loop #2	4.4/35	

PULL-IN RANGE

	+ Frequency	- Frequency
Loop #1	> 1KHz (1800Hz)	> 1KHz
Loop #2	> 400 Hz	> 400Hz at -120 dbm

AGC RESPONSE TIME

0.3 Seconds

Test Data Recorded By:

A T Mayle, Jr.

K. E. Cronkwright

Date: Feb. 15, 1964

15151 Bledsoe Street
San Fernando, California
telephone EMpire 7-2211

Federal LABORATORIES

Chicago
Fort Wayne
Palo Alto
San Fernando
Nutley

AROD FINAL TEST DATA

Channel # 3

REQUIRED REFERENCES (Inputs)

To J-12	Frequency	4.684 MHz
	Level	-2 dbm
To J-11	Frequency	19.4386
	Level	-6 dbm
To J-6	Frequency	70.26 MHz
	Level	+10 dbm
To J-9	Frequency	140.52 MHz
	Level	+6.4 dbm

NOTE: Tests performed on this channel without use of Module 11 (1st IF Amplifier). Therefore all signal levels are those into Module 1 (2nd mixer) and are 53 db above equivalent input to module 11. However, the noise, which is due to the amplified input noise of Module 11 is not present. So results are not same as when Module 11 is used. For example: When Module 11 is used, phase lock is lost on weak signals due to phase noise. When Module 11 is not used, phase lock is lost due to insufficient signal level, rather than phase noise.

SPECTRUM SIDETONE LEVELS

High Frequency Carrier	0	db
Low Frequency Carrier	-6	db
73 MHz Sideband	-7	db *
1.179 KHz Sideband	-4	db *
1.107 KHz Sideband	-4	db *

* Measured at J-4 on Module No. 2, with respect to the 2.342 MHz signal.

RANGE TONE OUTPUTS

At J-17 Frequency 2.342 MHz

Level 2.0 V. Peak-to-Peak with 50-Ω load

At J-13 Frequency 73.1875 KHz

Level 2.3 V. Peak-to-Peak. Max Set at 2.0 V. P-P

At J-15 Frequency 2.2871 KHz

Level 7 V. Peak-to Peak average level. Set at 2.0 V. P-P Avg. level.

At J-16 Frequency 71.47 Hz

Level 2 V. Peak-to-Peak Max

Signal at J4 of Module 8 Set for 5.0 V. P-P output (R91) with the 1.107, and 1.179 KHz Modulation applied. With 73 KHz Modulation, this level was 0.5 V. P-P.

DOPPLER SIGNAL OUTPUT

At J-7 Frequency 2.5 Hz to 1.6 MHz

Level 2.0V ± -6db at 1.6MHz

This excessive dropoff at 1.6 MHz is believed to be due to Low reference at 140.52 MHz.

DOPPLER POLARITY OUTPUT

At J-1 - R

Volts	Freq. A J-2 on A-5	4.684 MHz Loop Freq. Meter KHz
+9	84,1674 MHZ	-153 (est)
0	84,3188 MHZ	0
-9	84,5272 MHZ	+156 KHZ (est)
-6.1	84.452 MHz	+136 KHZ
+0.36	84.312 MHz	- 4.5 KHZ
+8.75	84.172 MHz	- 144 KHZ

Scale Max is ± 150 KHZ

VIDEO OUTPUT (3.7.2) * (~~50%~~ 100 % square Wave Modulation of 73 KHz)

Amplitude of 1 KHz Video @ J-14 8 V. Max Peak-to-Peak Set For 5.5V p-p

ACQUISITION SIGNAL (3.7.3) *

Level Acquired - 104

Level Unacquired - 105

Module II not available

MONITOR POINTS (3.8) *

Module II not available

a. AGC Voltage at J-1 - G

vs Signal into Module ~~II~~ I

Input	Volts at J-1-6	AGC Meter
-40 ~~-143~~ dbm	3.80	3.43
-50 ~~-142~~	3.60	3.27
-60 ~~-140~~	3.35	3.10
-70 ~~-135~~	2.95	2.87
-80 ~~-130~~	2.55	2.47
-85 ~~-125~~	2.40	2.20

(Table continued on next page)

* Refers to AROD-SPEC-9, Dated 26 August 1963

VS Signal into Module 11 (Cont.)

	Input	Volts at J-1-6	AGC Meter
-90	~~-120~~ dbm	1.74	1.80
-95	~~-115~~	1.05	1.25
-98	~~-110~~	0.18	0.60
-100	~~-105~~	0	0.15
	~~-100~~		
	~~-95~~		

b. Acquisition Signal at J-1-M

Not Acquired 0.0 V.

Acquired +4.8V.

c. Noise Analog Signal at J-1-L

Input	
~~-140~~ dbm	-95 dbm + 0.32V
130	-85 dbm & Stronger 0.08V.
120	
110	
100	
90	
80	

} Due to not using Module 11

d. Signal-to-Noise Ratio

Adjust R-13-A4 to switch at designated input levels.

Input Level	On Level	Off Level
~~140~~	-92dbm	-93dbm -91dbm
110		
125		

Module 11 Not used.

(Leave set at -125 dbm)

Output Voltages

	J1-J	J1-K
ON	5.07	5.07
OFF	0.06	0.06

e. VCO 2 Voltage at J-1-H

J-1-H Volts	Frequency	TP3A7 Volts	2.342 MHz Loop Freq. Meter
+1.8 V.	2.342 MHz	-0.5	+85 Hz
+2.28	2.341917	0	0
-0.37	2.342400	-2.78	+490 Hz
+4.1	2.341600	+1.18	-330 Hz

INPUT POWER

+18 VDC 560 ma

-18 VDC 451 ma

SENSITIVITY

Lowest level to Module 11 where phase-lock Loop #1 stays locked -_____dbm

Module 11 Not Available

(continued next page)

Lowest level to Module 11 where Loop #2 stays locked Module 11 Not Available

-_____dbm

Lowest level to Module 1 where Loop #1 stays locked

-104 dbm (2.05 V correlation)

Lowest level to Module 1 where Loop #2 stays locked

-92 dbm (0.5 V correlation)

CORRELATION METERS

RF Level ~~11~~ 1 To Module	4.684 MHz Loop Corr. Meter	2.342 MHz Loop Corr. Meter
-40 ~~-90~~ dbm	3.90	3.55
-50 ~~-100~~	3.90	3.95
-60 ~~-110~~	3.90	3.95
-70 ~~-120~~	3.90	3.85
-80 ~~-130~~	3.90	3.63
-85 ~~-135~~	3.90	2.83
-90 ~~-140~~	3.90	0.75
-95 ~~-142~~	3.87	0
-98 ~~-143~~	3.85	0
-100 ~~-144~~	3.63	0

NOTE: Relationship of main carrier to modulated carrier (2.342 MHz below main carrier) at input to Module ~~11~~ 1 is

6 db.

PHASE-LOCK LOOP BANDWIDTHS

	3 db BW	Calculated RF Noise BW
Loop #1	31 Hz	96 Hz
Loop #2	3.5/35 Hz	11/110 Hz

3db BW Taken as point where phase shift is 90°. (ie Phase Detector output Vs Function Gen, Input to Phase Modulator)

PULL-IN RANGE

	+ Frequency	- Frequency
Loop #1	> 1000 Hz	> 1000 Hz
Loop #2	> 500 Hz	> 500 Hz

With -80 dbm input to Module A1.

AGC RESPONSE TIME

0.3 Seconds

Input about -50 dbm to Module 1

Test Data Recorded By:

Roy E. Cronkinwright
AT Maple

Date: 3/11/69